EC200G-CN

Hardware Design

LTE Standard Module Series

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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any terminal or mobile incorporating the module. Manufacturers of the terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other terminals. Areas with explosive or potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2023-04-27	Denny QIN/ Kleene QIN/ Kevin WANG	Creation of the document
1.0	2023-10-23	Denny QIN/ Kleene QIN/ Kevin WANG	First official release
1.1	2024-03-14	Denny QIN/ Kleene QIN/ Kevin WANG	1. Added a note on VBAT voltage requirement before the module's power-on (Chapter 3.5.1). 2. Added a note on RESET_N (Chapter 3.7). 3. Added a note on UART hardware flow control design (Chapter 4.4). 4. Added GNSS design principles (Chapter 5.3.3). 5. Deleted GNSS active antenna gain (Table 35).

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1 Introduction

This document describes the EC200G-CN module and its hardware interfaces and air interfaces connected to your applications. It provides a quick insight into the module's information such as interface specifications, RF performance, electrical and mechanical specifications.

1.1. Special Marks

Table 1: Special Marks

Mark	Definition
*	Unless otherwise specified, an asterisk (*) after a function, feature, interface, pin name, command, argument, and so on indicates that it is under development and currently not supported; and the asterisk (*) after a model indicates that the model sample is currently unavailable.
[…]	Brackets ([…]) used after a pin enclosing a range of numbers indicate all pins of the same type. For example, SDIO_DATA[0:3] refers to all four SDIO pins: SDIO_DATA0, SDIO_DATA1, SDIO_DATA2, and SDIO_DATA3.

2 Product Overview

EC200G-CN is an SMD module with compact packaging, which is engineered to meet most of the demands of M2M applications.

Table 2: Basic Information

EC200G-CN	
Packaging type	LCC + LGA
Pin counts	144 pins
Dimensions	(28.0 ±0.15) mm × (31.0 ±0.15) mm × (2.4 ±0.2) mm
Weight	Approx. 3.75 g

2.1. Frequency Bands and Functions

Table 3: Frequency Bands and Functions

Wireless Network Type	EC200G-CN
LTE-FDD	B1/B3/B5/B8
LTE-TDD	B34/B38/B39/B40/B41 (140 MHz)
GNSS	GPS/BDS/QZSS
Wi-Fi Scan	2.4 GHz 11b (Rx)
Bluetooth	Optional

NOTE

GNSS and Bluetooth functions of the module are optional. For more details, contact Quectel Technical Support.

2.2. Key Features

Table 4: Key Features

Category	Description
Supply Voltage	● 3.3–4.3 V ● Typical: 3.8 V
USB Interface	● Complies with USB 2.0 specification (slave mode only) ● Data rate: up to 480 Mbps ● Used for AT command communication, data transmission, software debugging and firmware upgrade ● Supports USB serial drivers for Windows 8/8.1/10/11, Linux 2.6–6.7 and Android 4.x–13.x systems
Forced Download Interface	Supports one forced download interface
USIM Interface [1]	Supports 1.8 V and 3.0 V
UART	**Main UART:** ● Used for AT command communication and data transmission ● Baud rate: Max. 2 Mbps, 115200 bps by default ● Supports RTS and CTS hardware flow control **Debug UART:** ● Used for AP log output ● Baud rate: 2 Mbps by default ● Cannot be used as a general UART **Auxiliary UART:** ● Used for data transmission ● Baud rate: Max. 2 Mbps, 115200 bps by default
Analog Audio Features (Optional) [2]	● Supports one analog audio input and one analog audio output channels ● Supports echo cancellation and noise suppression

[1] The USIM2 interface of the module is optional. If the hardware supports USIM2 interface, Dual SIM Dual Standby or Dual SIM Single Standby can be enabled through software configuration. For more details, contact Quectel Technical Support.
[2] There are pin conflicts among PCM interface, analog audio interface and PWM audio interface functions, and choose one of the three functions for implementing the audio function.

PCM Interface (Optional) [2]	Supports master mode
PWM Audio Interface (Optional) [2]	Supports PWM playback of audio files/streams (recording is not supported)
I2C Interfaces	● Supports two I2C interfaces ● Comply with the I2C-bus Specification
ADC Interfaces	Supports three ADC interfaces
Network Indication	● NET_MODE indicates the network registration mode ● NET_STATUS indicates network activity status
Antenna Interfaces	● LTE/Wi-Fi Scan antenna interface (ANT_MAIN/WIFI_SCAN) [3] ● Bluetooth antenna interface (ANT_BT) (optional) ● GNSS antenna interface (ANT_GNSS) (optional) ● 50 Ω characteristic impedance
SMS	● Text and PDU mode ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: USIM card and ME, ME by default
AT Commands	● Comply with *3GPP TS 27.007* and *3GPP TS 27.005* ● Comply with Quectel enhanced AT commands
Transmitting Power	● LTE-FDD: Class 3 (23 dBm ±2 dB) ● LTE-TDD: Class 3 (23 dBm ±2 dB)
LTE Features	● Supports up to 3GPP Rel-13 Cat 1 bis FDD and TDD ● Supports 1.4/3/5/10/15/20 MHz RF bandwidths ● LTE-FDD max. data rates: – DL: 10 Mbps – UL: 5 Mbps ● LTE-TDD max. data rates: – DL: 8.96 Mbps – UL: 3.1 Mbps ● Supports UL QPSK and 16QAM modulations ● Supports DL QPSK, 16QAM and 64QAM modulations
Internet Protocol Features [4]	● Complies with TCP/UDP/PPP/NTP/NITZ/FTP/HTTP/PING/CMUX/ HTTPS/FTPS/SSL/FILE/MQTT/SMTP/SMS/MMS/SMTPS protocols ● Supports PAP and CHAP for PPP connections
Temperature Ranges	● Normal operating temperature [5]: -35 °C to +75 °C ● Extended operating temperature [6]: -40 °C to +85 °C

[3] Wi-Fi Scan shares the same antenna interface with the main antenna. The two functions cannot be used at the same time, and Wi-Fi Scan only supports receiving.
[4] FTP, FTPS, MMS, SMTP and SMTPS protocols are optional.
[5] Within this range, the module's indicators comply with 3GPP specification requirements.
[6] Within this range, the module retains the ability to establish and maintain functions such as voice*, SMS, data transmission and emergency call*, without any unrecoverable malfunction. Radio spectrum and radio network remain uninfluenced, whereas the value of one or more parameters, such as P_{out}, may decrease and fall below the range of the 3GPP specified tolerances. When the temperature returns to the normal operating temperature range, the module's indicators will comply with 3GPP specification requirements again.

	• Storage temperature: -40 °C to +90 °C
Firmware Upgrade	Via USB interface or FOTA
RoHS	All hardware components are fully compliant with EU RoHS directive

2.3. Functional Diagram

The functional diagram illustrates the following major functional parts:

- Baseband part
- Radio frequency part
- Peripheral interfaces

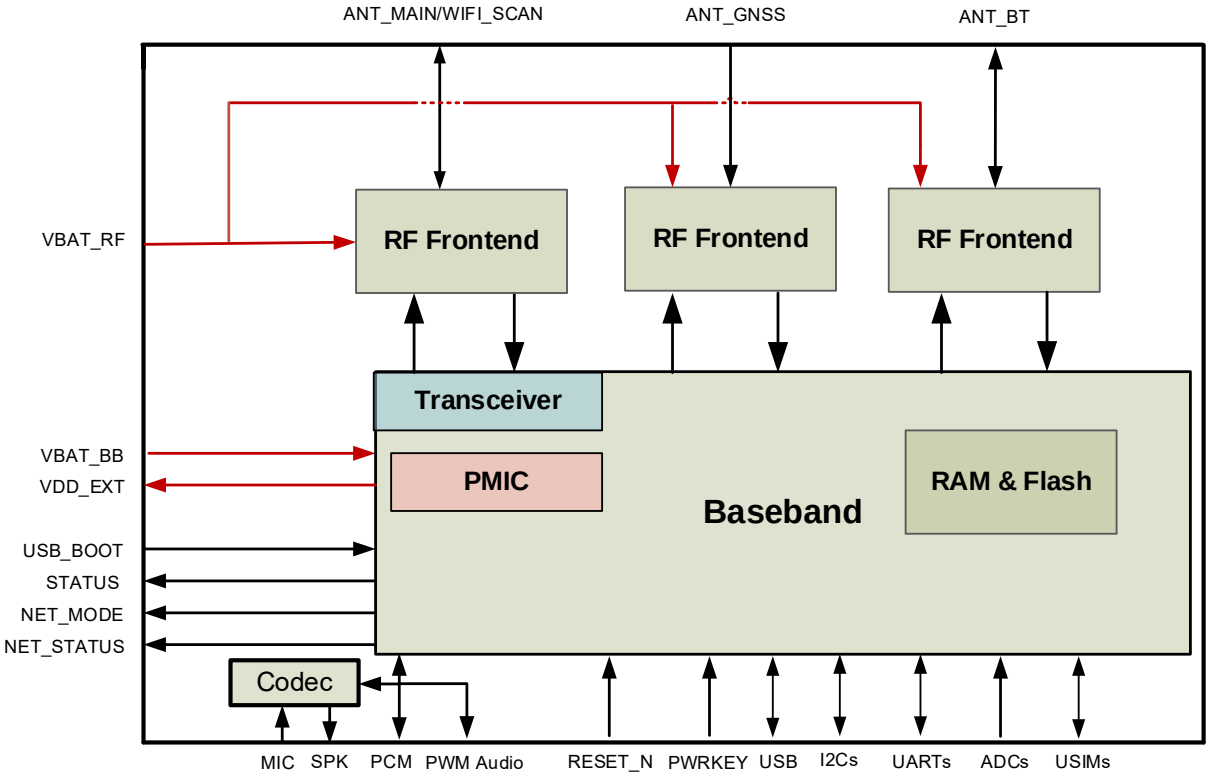


Figure 1: Functional Diagram

NOTE

1. There are pin conflicts among PCM interface, analog audio interface and PWM audio interface functions, and choose one of the three functions for implementing the audio function.
2. GNSS, Bluetooth and USIM2 functions of the module are all optional. For more details, contact Quectel Technical Support.

2.4. Pin Assignment

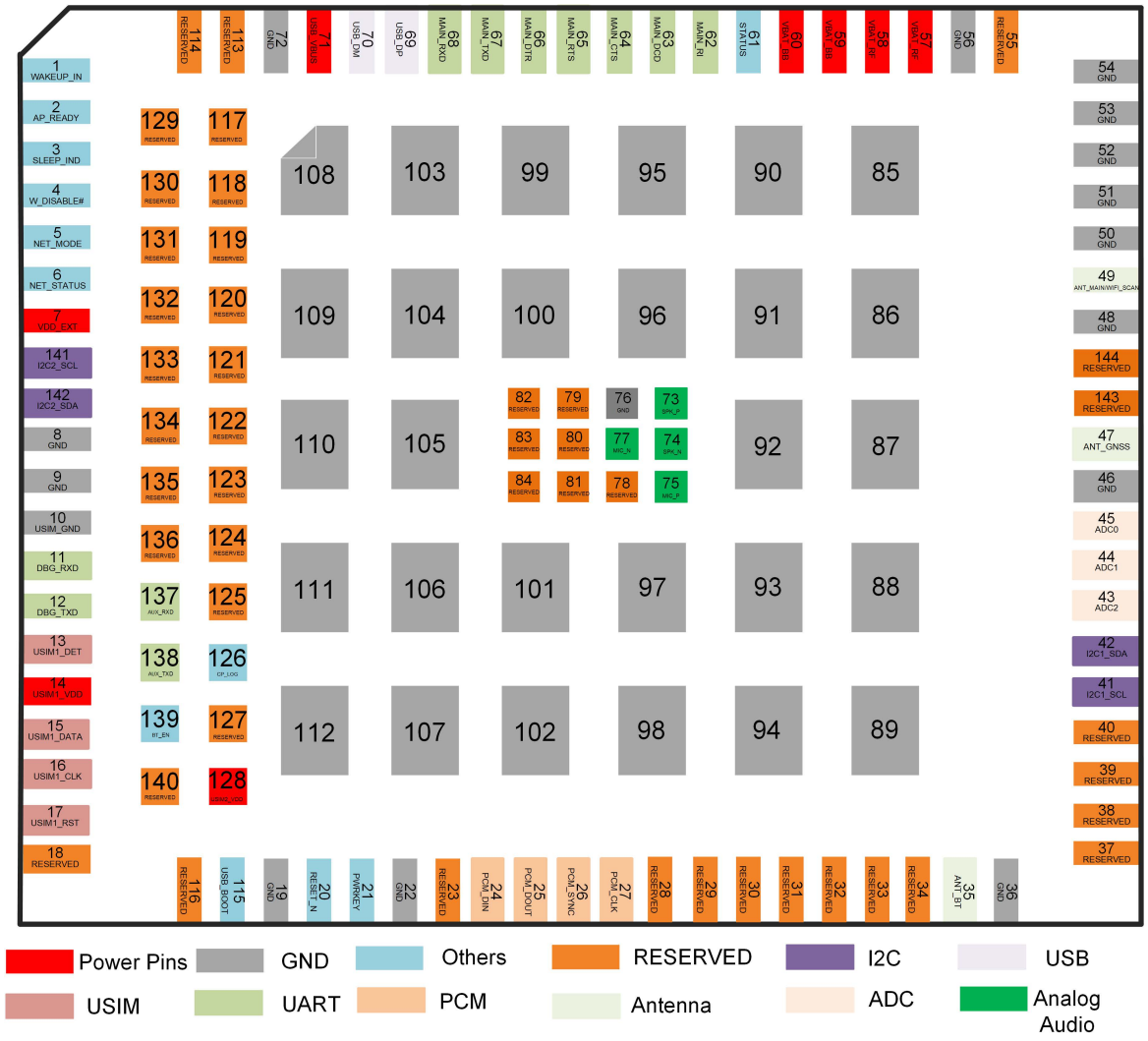


Figure 2: Pin Assignment (Top View)

NOTE

1. Keep all RESERVED pins and unused pins open. All GND pins should be connected to ground.
2. If forced download function is not used, do not pull USB_BOOT to low level or high level and keep this pin open before the module is successfully turned on.
3. There are pin conflicts among PCM interface, analog audio interface and PWM audio interface functions, and choose one of the three functions for implementing the audio function.
4. GNSS, Bluetooth and USIM2 functions of the module are all optional. For more details, contact Quectel Technical Support.
5. If the selected module model supports Bluetooth function, pin 117 can be used for Bluetooth log output. For more details, contact Quectel Technical Support.

2.5. Pin Description

Table 5: Parameter Definition

Parameter	Description
AI	Analog Input
AIO	Analog Input/Output
AO	Analog Output
DI	Digital Input
DIO	Digital Input/Output
DO	Digital Output
OD	Open Drain
PI	Power Input
PO	Power Output

DC characteristics include power domain and rated current.

Table 6: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	59, 60	PI	Power supply for module's baseband part	Vmin = 3.3 V Vnom = 3.8 V Vmax = 4.3 V	External power supply must be provided with sufficient current of at least 1.5 A. It is recommended to add a TVS externally. A test point is recommended to be reserved.
VBAT_RF	57, 58	PI	Power supply for module's RF part		External power supply must be provided with sufficient current of at least 2 A. It is recommended to add a TVS externally. A test point is recommended to be reserved.
VDD_EXT	7	PO	Provide 1.8 V for external circuit	Vnom = 1.8 V $I_O$max = 50 mA	Power supply for external GPIO's pull-up circuits. Add 2.2 μF capacitor and TVS components if used. A test point is recommended to be reserved.
GND	8, 9, 19, 22, 36, 46, 48, 50–54, 56, 72, 76, 85–112				
Turn On/Off/Reset					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	21	DI	Turn on/off the module	VBAT power domain V_{IL}max = 0.5 V	A test point is recommended to be reserved.
RESET_N	20	DI	Reset the module		Active low.

					A test point is recommended to be reserved if unused.
Indication Signals					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
NET_STATUS	6	DO	Indicate the module's network activity status	1.8 V	If unused, keep them open.
NET_MODE	5	DO	Indicate the module's network registration mode		
STATUS	61	DO	Indicate the module's operation status		
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	71	AI	USB connection detect	Vmin = 3.5 V Vnom = 5.0 V Vmax = 5.25 V	Typical: 5.0 V. A test point must be reserved. The USB_VBUS pin needs to be connected with a 1 kΩ resistor in series if USB_VBUS is connected to power supply and VBAT is powered down.
USB_DP	69	AIO	USB 2.0 differential data (+)		90 Ω differential impedance is required. Test points must be reserved.
USB_DM	70	AIO	USB 2.0 differential data (-)		
USIM Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM1_VDD	14	PO	USIM1 card power supply	1.8/3.0 V	Either 1.8 V or 3.0 V USIM card is supported and can be identified automatically by the module.

USIM1_DATA	15	DIO	USIM1 card data		
USIM1_CLK	16	DO	USIM1 card clock		
USIM1_RST	17	DO	USIM1 card reset		
USIM1_DET	13	DI	USIM card hot-plug detect	1.8 V	If unused, keep it open.
USIM_GND	10	-	Specified ground for USIM card		Connect to the ground of USIM card connector.
USIM2_VDD	128	PO	USIM2 card power supply	1.8/3.0 V	Either 1.8 V or 3.0 V USIM card is supported and can be identified automatically by the module.
Main UART					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MAIN_CTS	64	DO	Clear to send signal from the module	1.8 V	Connect to MCU's CTS. If unused, keep it open.
MAIN_RTS	65	DI	request to send signal to the module		Connect to MCU's RTS. If unused, keep it open.
MAIN_RXD	68	DI	Main UART receive		If unused, keep them open.
MAIN_DCD	63	DO	Main UART data carrier detection		
MAIN_TXD	67	DO	Main UART transmit		
MAIN_RI	62	DO	Main UART ring indication		
MAIN_DTR	66	DI	Main UART data terminal ready		
Auxiliary UART					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
AUX_TXD	138	DO	Auxiliary UART transmit	1.8 V	If unused, keep them open.
AUX_RXD	137	DI	Auxiliary UART		

			receive		
Debug UART					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_RXD	11	DI	Debug UART receive	1.8 V	Test points must be reserved.
DBG_TXD	12	DO	Debug UART transmit		
RF Antenna Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_MAIN/WIFI_SCAN	49	AIO/AI	LTE/Wi-Fi Scan antenna interface		50 Ω characteristic impedance.
ANT_BT	35	AIO	Bluetooth antenna interface		50 Ω characteristic impedance.
ANT_GNSS	47	AI	GNSS antenna interface		If unused, keep them open. GNSS and Bluetooth functions of the module are optional.
ADC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC0	45	AI	General-purpose ADC interface	Input voltage range: 0–VBAT	Use a 1 kΩ resistor in series. If a voltage divider resistor is used, the external voltage divider resistor must be less than 100 kΩ. If unused, keep them open.
ADC1	44	AI			
ADC2	43	AI			
Forced Download Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_BOOT	115	DI	Force the module into forced download mode	1.8 V	Active low. If the forced download function is not used, do not pull it to low level or high level and keep it

					open before the module is successfully turned on. A test point is recommended to be reserved.
Analog Audio Interface (Optional)					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SPK_P	73	AO	Analog audio differential output (+)		
SPK_N	74	AO	Analog audio differential output (-)		
MIC_P	75	AI	Microphone analog input (+)		
MIC_N	77	AI	Microphone analog input (-)		
I2C Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2C1_SCL	41	OD	I2C1 serial clock	1.8 V	An external 1.8 V pull-up resistor is needed. If unused, keep them open.
I2C1_SDA	42	OD	I2C1 serial data		
I2C2_SCL	141	OD	I2C2 serial clock		
I2C2_SDA	142	OD	I2C2 serial data		
PCM Interface (Optional)					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCM_DIN	24	DI	PCM data input	1.8 V	Only supports master mode. If unused, keep them open.
PCM_DOUT	25	DO	PCM data output		
PCM_SYNC	26	DO	PCM data frame sync		
PCM_CLK	27	DO	PCM clock		
Other Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

WAKEUP_IN	1	DI	Wake up the module	If unused, keep them open.
AP_READY	2	DI	Application processor ready	
SLEEP_IND	3	DO	Sleep indicator	
W_DISABLE#	4	DI	Airplane mode control	Pull-up by default. Driving the pin low can make the module enter the airplane mode. If unused, keep it open.
CP_LOG	126	DO	CP log output	It can output CP log, and only 8 Mbps baud rate is supported. A test point must be reserved.
BT_EN	139	DO	Bluetooth enable control	1.8/3.2 V, 1.8 V by default. If unused, keep it open.
RESERVED pins				
Pin Name	**Pin No.**			**Comment**
RESERVED	18, 23, 28–34, 37–40, 55, 78–84, 113, 114, 116–125, 127,129–136, 140, 143, 144			Keep them open.

NOTE

USIM2 function is optional for the module. For more details, contact Quectel Technical Support.

2.6. EVB Kit

Quectel supplies an evaluation board (UMTS&LTE EVB) with accessories to develop and test the module. For more details, see ***document [1]***.

3 Operating Characteristics

3.1. Operating Modes

Table 7: Operating Mode Overview

Mode	Description	
Full Functionality Mode	Idle	The module remains registered on the network but has no data interaction with the network. In this mode, the software is active.
	Voice*/Data	The module is connected to the network. In this mode, the power consumption is decided by network settings and data rates.
Minimum Functionality Mode	**AT+CFUN=0** can set the module to the minimum functionality mode without removing the power supply. In this case, both RF function and USIM card are disabled.	
Airplane Mode	**AT+CFUN=4** or pulling down W_DISABLE# can set the module into airplane mode. In this case, RF function is disabled.	
Sleep Mode	The module can still receive paging*, SMS, voice call* and TCP/UDP data from the network. In this mode, the power consumption is reduced to an ultra-low level.	
Shutdown Mode	In this mode, software is not active. However, operating voltage connected to VBAT remains applied.	

NOTE

For more details about **AT+CFUN**, see ***document [2]***.

3.2. Sleep Mode

With DRX technology, power consumption of the module will be reduced to an ultra-low level.

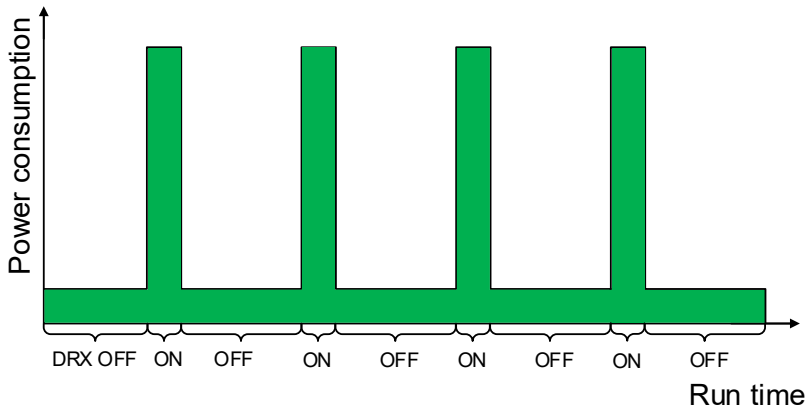


Figure 3: Module Power Consumption in Sleep Mode

NOTE

DRX cycle values are transmitted over the wireless network.

3.2.1. UART Application Scenario

If the module communicates with the MCU via main UART, both the following preconditions should be met to set the module to sleep mode:

- Execute **AT+QSCLK=1** to enable sleep mode. For more details, see ***document [3]***.
- Ensure MAIN_DTR is held high or kept open.

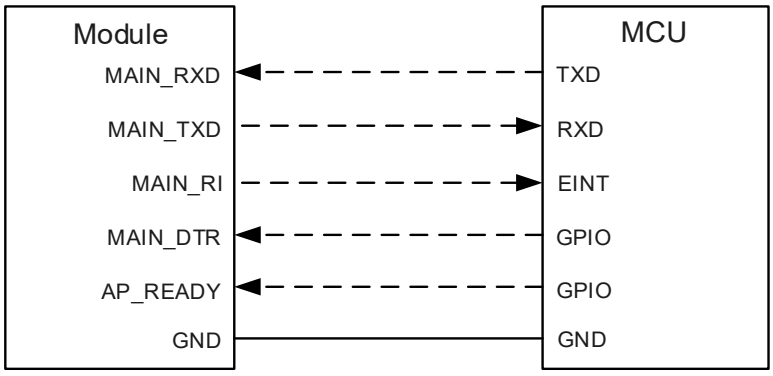


Figure 4: Block Diagram of UART Application in Sleep Mode

- Driving MAIN_DTR low with the MCU will wake up the module.
- When the module has a URC to report, MAIN_RI signal will wake up the MCU. See ***Chapter 4.9.3*** for details about MAIN_RI behavior.

3.2.2. USB Application Scenarios

For the two scenarios in ***Chapters 3.2.2.1*** and ***3.2.2.2*** below, three preconditions must be met to set the module to sleep mode:

- Execute **AT+QSCLK=1** to enable sleep mode.
- Ensure MAIN_DTR is held high or is kept open.
- Ensure the host's USB bus, which is connected to the module's USB interface, enters Suspend state.

3.2.2.1. USB Application with USB Remote Wakeup Function

If the host supports USB Suspend/Resume and remote wakeup function, the following figure shows the connection between the module and the host.

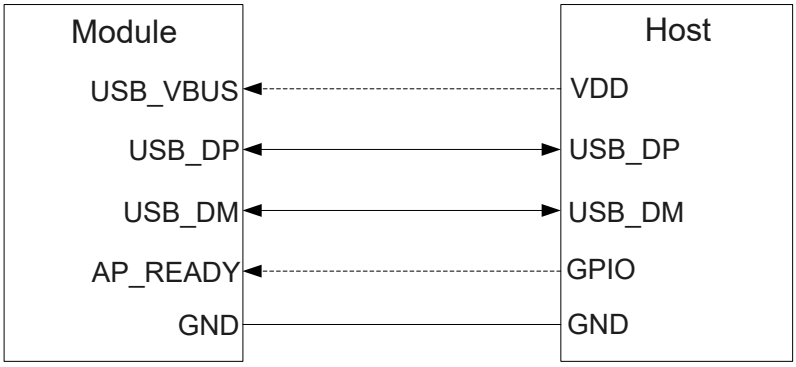


Figure 5: Block Diagram of Application with USB Remote Wakeup Function in Sleep Mode

- Sending data to the module through USB will wake up the module.
- When the module has a URC to report, the module will send remote wake-up signals through USB bus to wake up the host.

3.2.2.2. USB Application with USB Suspend/Resume and MAIN_RI Function

If the host supports USB Suspend/Resume, but does not support remote wakeup function, the MAIN_RI signal is needed to wake up the host.

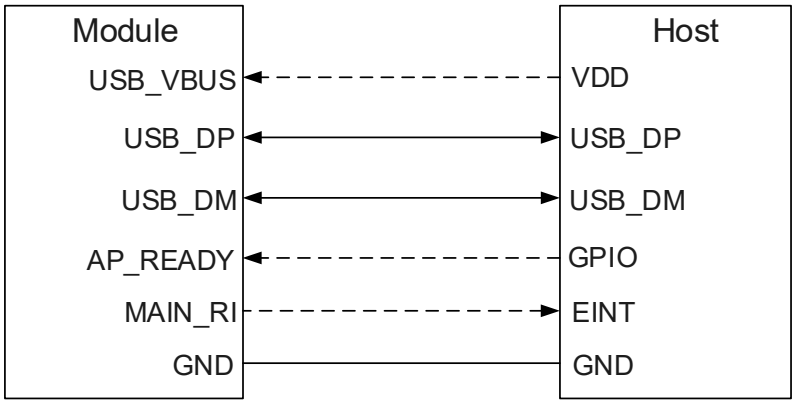


Figure 6: Block Diagram of Application with MAIN_RI Function in Sleep Mode

- Sending data to the module through USB will wake up the module.
- When the module has a URC to report, the module will wake up the host through MAIN_RI signal. See ***Chapter 4.9.3*** for details about MAIN_RI.

3.2.2.3. USB Application Without USB Suspend Function

If the host does not support USB Suspend function, the following three preconditions must be met to set the module to sleep mode:

- Execute **AT+QSCLK=1** to enable sleep mode.
- Ensure MAIN_DTR is held high or is kept open.
- Ensure USB_VBUS is disconnected via the external control circuit.

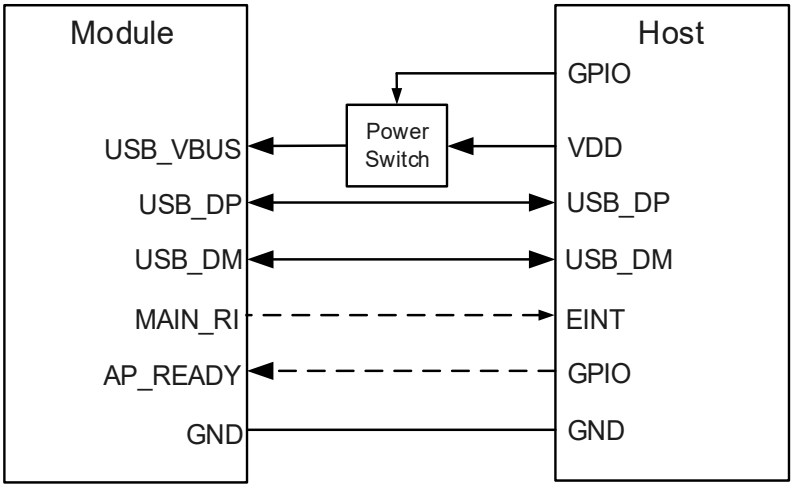


Figure 7: Block Diagram of Application Without USB Suspend Function in Sleep Mode

Restoring the power supply of USB_VBUS will wake up the module.

NOTE

1. Pay attention to the level match shown in the dotted line between the module and the MCU/host.
2. USB Suspend is supported on the Linux system, but not on the Windows system.

3.3. Airplane Mode

When the module enters airplane mode, the RF function does not work and all AT commands related to the RF function are inaccessible. The following ways can be used to let the module enter airplane mode.

Hardware:

The W_DISABLE# pin is pulled up by default. Its control function for airplane mode is disabled by default and **AT+QCFG="airplanecontrol",1** can be used to enable the function. Driving the pin low after its control function for airplane mode is enabled by AT command can make the module enter the airplane mode.

Software:

AT+CFUN=<fun> provides the choice of the functionality level through setting **<fun>** into 0, 1 or 4.

- **AT+CFUN=0:** Minimum functionality mode (RF and USIM functions disabled).
- **AT+CFUN=1:** Full functionality mode (by default).
- **AT+CFUN=4:** Airplane mode (RF function disabled).

NOTE

For more details about the above-mentioned AT command, see ***document [2]***.

3.4. Power Supply

3.4.1. Power Supply Interfaces

The module provides four VBAT pins for connection with the external power supply.

Table 8: Pin Definition of Power Supply Interfaces

Pin Name	Pin No.	I/O	Description	Comment
VBAT_RF	57, 58	PI	Power supply for module's RF part	External power supply must be provided with sufficient current of at least 2 A. It is recommended to add a TVS externally. A test point is recommended to be reserved.
VBAT_BB	59, 60	PI	Power supply for module's baseband part	External power supply must be provided with sufficient current of at least 1.5 A. It is recommended to add a TVS externally. A test point is recommended to be reserved.

3.4.2. Reference Design for Power Supply

Power design for the module is essential. The power supply of the module should be able to provide sufficient current of at least 2 A. If the voltage difference between input and output is small, it is suggested to use an LDO; if the voltage difference is big, a buck converter is recommended.

The figure below is a reference design for a 5 V supply circuit.

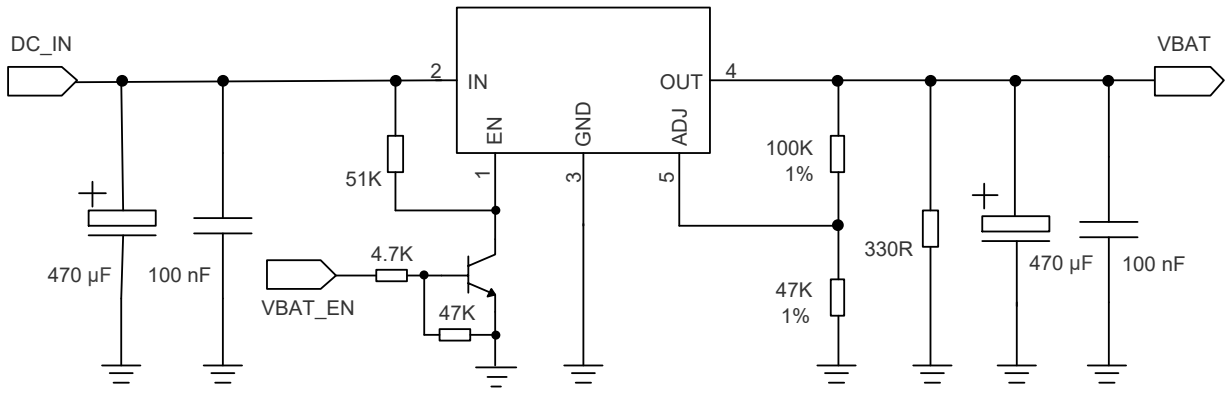


Figure 8: Reference Design of Power Input

3.4.3. Voltage Stability Requirements

The power supply range of the module is from 3.3 V to 4.3 V. Ensure the input voltage never drops below 3.3 V.

To decrease voltage drop, a filter capacitor of about 100 μF with low ESR (ESR ≤ 0.7 Ω) should be used, and a multi-layer ceramic chip (MLCC) capacitor array should also be reserved due to its ultra-low ESR. Use three ceramic capacitors (100 nF, 33 pF, 10 pF) and one 0 Ω resistor (the package should be at least 0603) for composing the MLCC array, and place these capacitors close to VBAT_BB and VBAT_RF pins. The main power supply from an external application has to be a single voltage source and can be expanded to two sub paths with star configuration routing. The width of VBAT_BB trace should not be less than 2 mm; and the width of VBAT_RF trace should not be less than 2.5 mm. In principle, the longer the VBAT trace is, the wider it should be.

To avoid the ripple and surge and to ensure the stability of the power supply to the module, add a high-power TVS at the front end of the power supply.

The following figure shows the star configuration routing of the power supply.

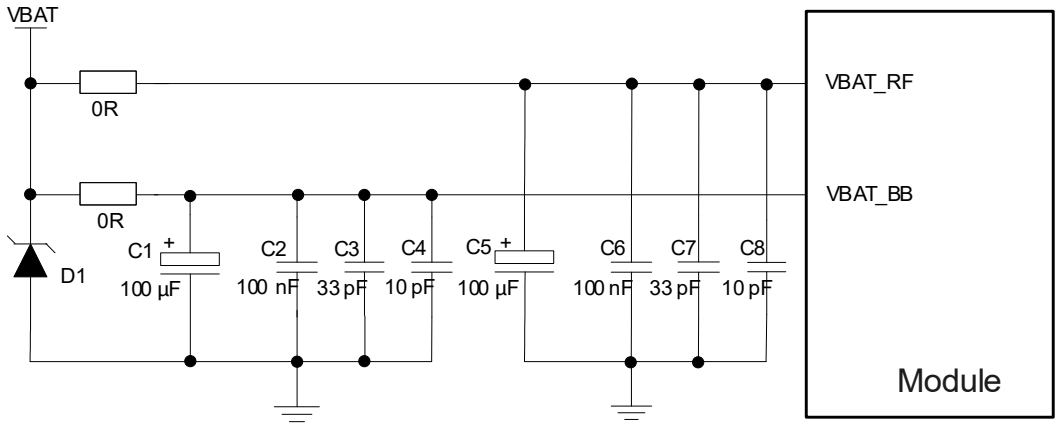


Figure 9: Power Supply in Star Configuration

3.5. Turn On

3.5.1. Turn On with PWRKEY

Table 9: Pin Definition of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	21	DI	Turn on/off the module	VBAT power domain. A test point is recommended to be reserved.

When the module is in turn-off state, it can be turned on by driving PWRKEY low for at least 2 s. It is recommended to use an open drain/collector driver to control the PWRKEY. A simple reference circuit is illustrated in the following figure.

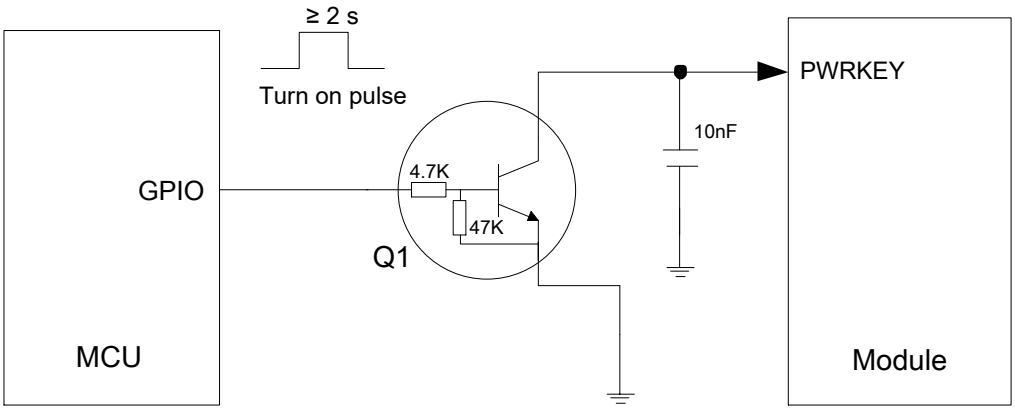


Figure 10: Reference Design of Turn-on with Driving Circuit

If the module needs to turn on automatically when powered up, but does not need turn-off function, PWRKEY can be driven low directly to ground with a recommended resistor of less than 1 kΩ.

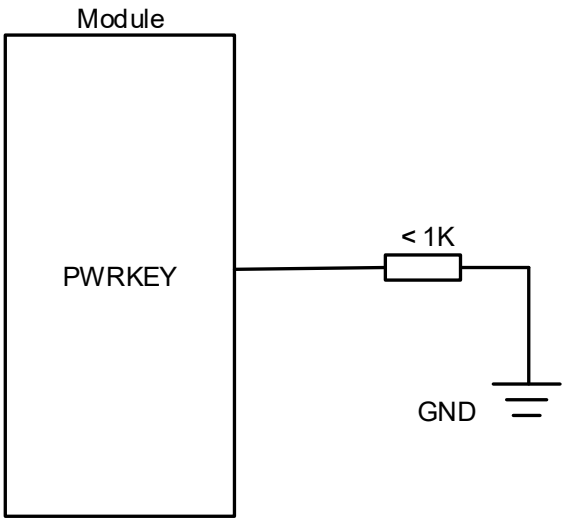


Figure 11: Reference Design of Automatic Turn-on upon Power-up

Another way to control the PWRKEY is using a button directly. When pressing the button, an electrostatic strike may be generated from finger. Therefore, you should place a TVS near the button for ESD protection.

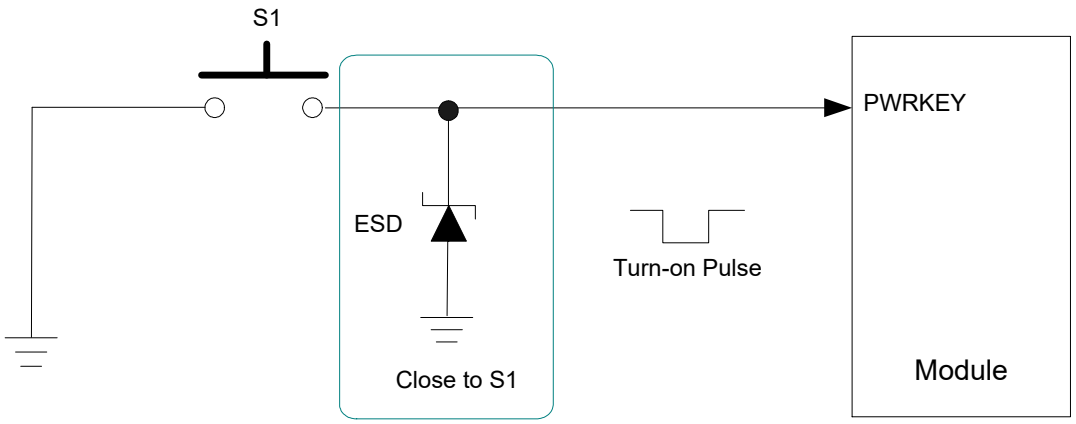


Figure 12: Reference Design of Turn-on with a Button

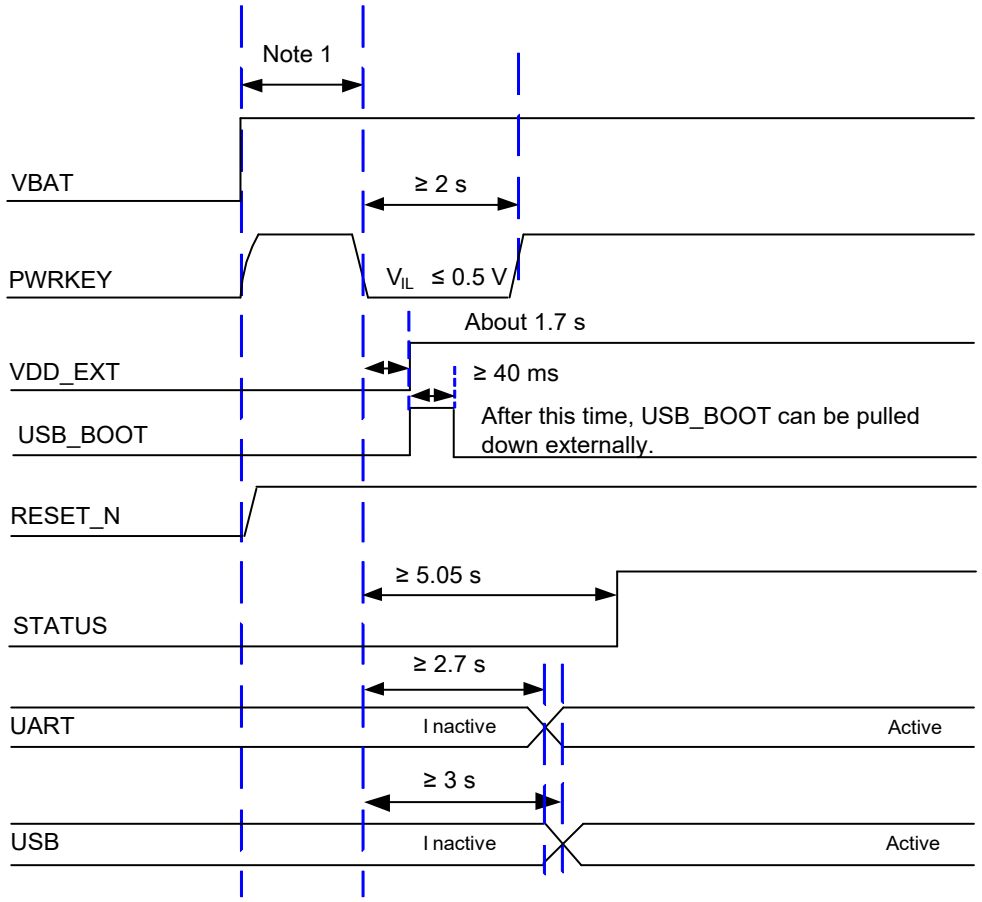


Figure 13: Timing of Turn-on with PWRKEY

NOTE

1. Ensure the voltage of VBAT is stable for at least 30 ms before driving the PWRKEY low.
2. Pay attention to the following two power-on scenarios:
   - In the scenario where USB_VBUS is connected first (or has always been connected), VBAT is powered on later, and then PWRKEY is pulled down to start up the module, it is necessary to ensure that VBAT is powered on stably for at least 2 s before PWRKEY is pulled down;
   - In the scenario where VBAT is powered on first (or has always been powered on), USB_VBUS is connected later, and then PWRKEY is pulled down to start up the module, it is necessary to ensure that USB_VBUS is connected for at least 2 s before PWRKEY is pulled down.
3. Ensure that the VBAT voltage is less than 0.5 V before powering up the module again. If MOSFET is used to control the VBAT power supply, a discharge circuit must be designed to ensure that the VBAT voltage can be released quickly after the module is shut down and powered off. If the peripheral watchdog circuit is reserved, it is recommended to control the VBAT power supply of the module with an on-off circuit.

3.6. Turn Off

3.6.1. Turn Off with PWRKEY

Drive PWRKEY low for at least 3 s and then release it to turn off the module.

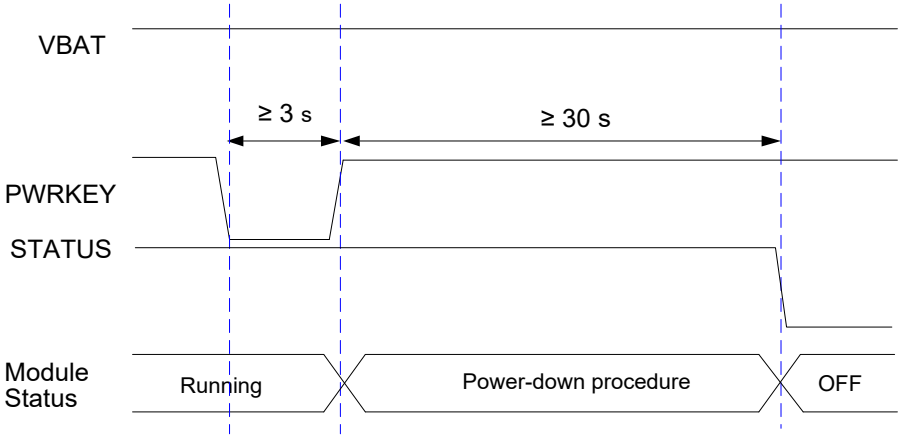


Figure 14: Turn-off Timing

3.6.2. Turn Off with AT Command

It is also a safe way to use **AT+QPOWD** to turn off the module, which is similar to the procedure of turning off the module via PWRKEY. See ***document [2]*** for details about **AT+QPOWD**.

NOTE

1. To avoid corrupting the data in the internal flash, do not switch off the power supply to turn off the module when the module works normally. Only after turning off the module with PWRKEY or AT command can you cut off the power supply.
2. When the PWRKEY pin has been kept pulled down directly to GND, the module will not boot automatically after being turned off with the AT command. In this case, it is necessary to forcibly disconnect the VBAT power supply and turn on the module again. Therefore, it is recommended to use a control circuit to control PWRKEY to turn on/off the module instead of keeping the PWRKEY connected to GND.
3. During the shutdown process, the time when the module logs out of the network is related to the current network status. Therefore, the specific shutdown time is affected by the network status, and attention should be paid to the shutdown time when designing.

3.7. Reset

Driving RESET_N low for at least 100 ms and then releasing it can reset the module. RESET_N signal is sensitive to interference, consequently it is recommended to route the trace as short as possible and surround it with ground.

Table 10: Pin Definition of RESET_N

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	20	DI	Reset the module	VBAT power domain. Active low. A test point is recommended to be reserved if unused.

The recommended circuit for reset function is similar to the PWRKEY control circuit. You can use an open drain/collector driver or a button to control RESET_N.

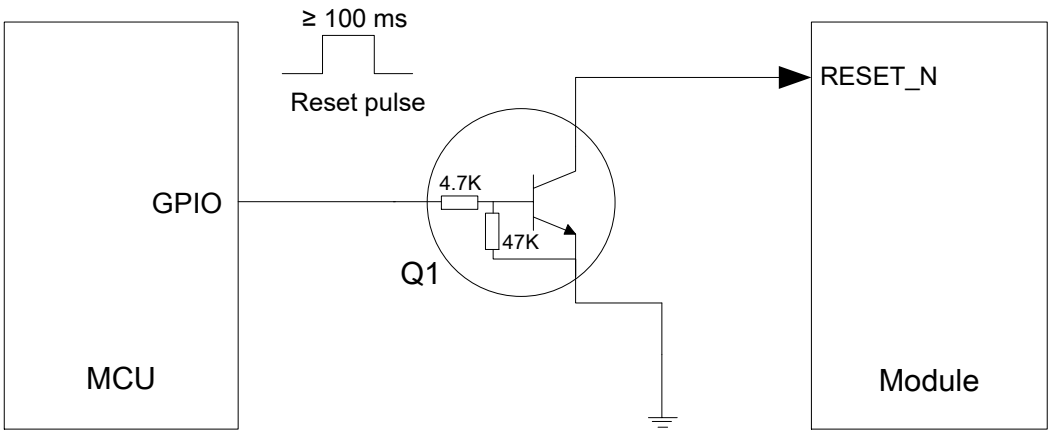


Figure 15: Reference Design of RESET_N with Driving Circuit

You can also use a button to control the RESET_N:

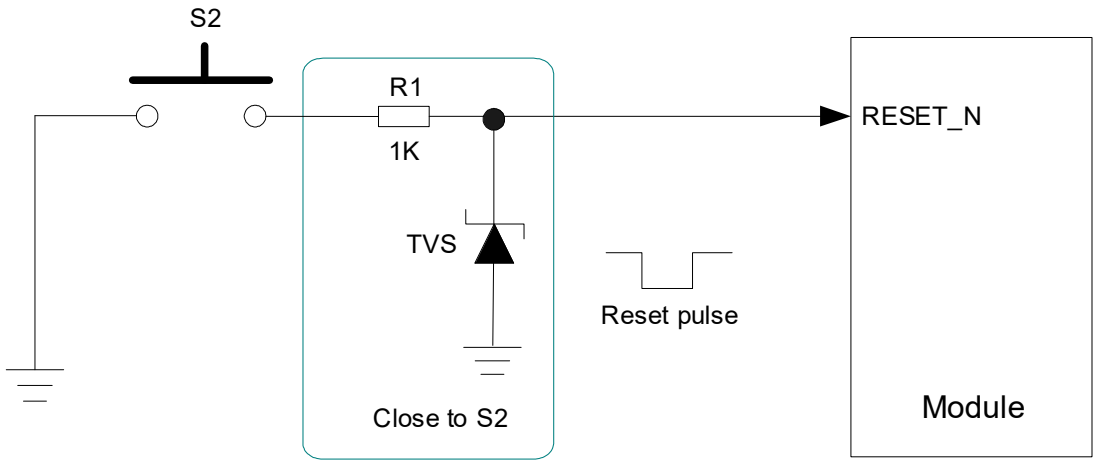


Figure 16: Reference Design of RESET_N with a Button

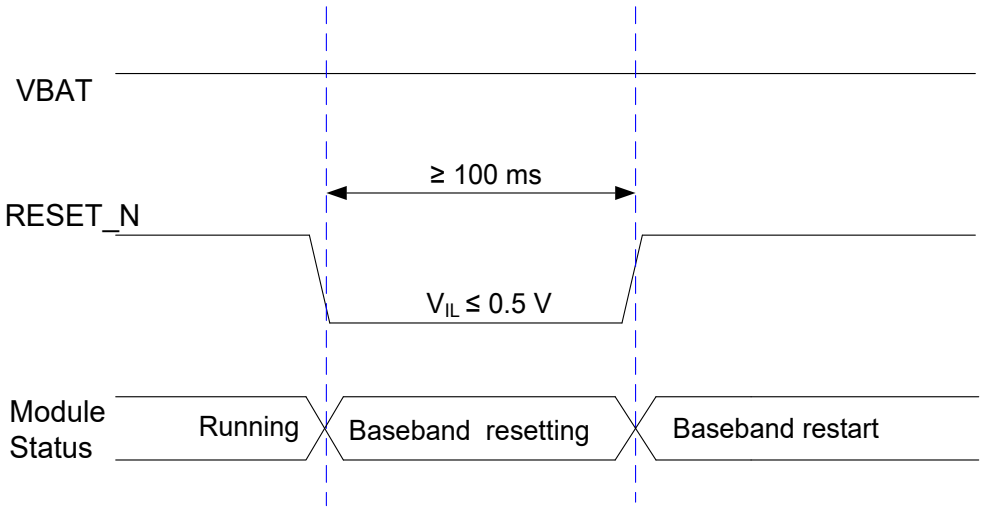


Figure 17: Timing of Reset

NOTE

1. Use RESET_N only when you fail to turn off the module with **AT+QPOWD** and PWRKEY.
2. Ensure the capacitance on PWRKEY and RESET_N does not exceed 10 nF.
3. The RESET_N pin performs a soft reset which only resets the baseband, not the PMU.

4 Application Interfaces

4.1. USB Interface

The module provides one USB interface which complies with the USB 2.0 specifications (slave mode only) and supports high-speed (480 Mbps) and full-speed (12 Mbps) for USB 2.0. The USB interface can be used for AT command communication, data transmission, software debugging and firmware upgrade.

Table 11: Pin Definition of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	71	AI	USB connection detect	Typical: 5.0 V. A test point must be reserved. The USB_VBUS pin needs to be connected with a 1 kΩ resistor in series if USB_VBUS is connected to power supply and VBAT is powered down.
USB_DP	69	AIO	USB 2.0 differential data (+)	90 Ω differential impedance is required. Test points must be reserved.
USB_DM	70	AIO	USB 2.0 differential data (-)	

Test points must be reserved for debugging and firmware upgrading in your designs.

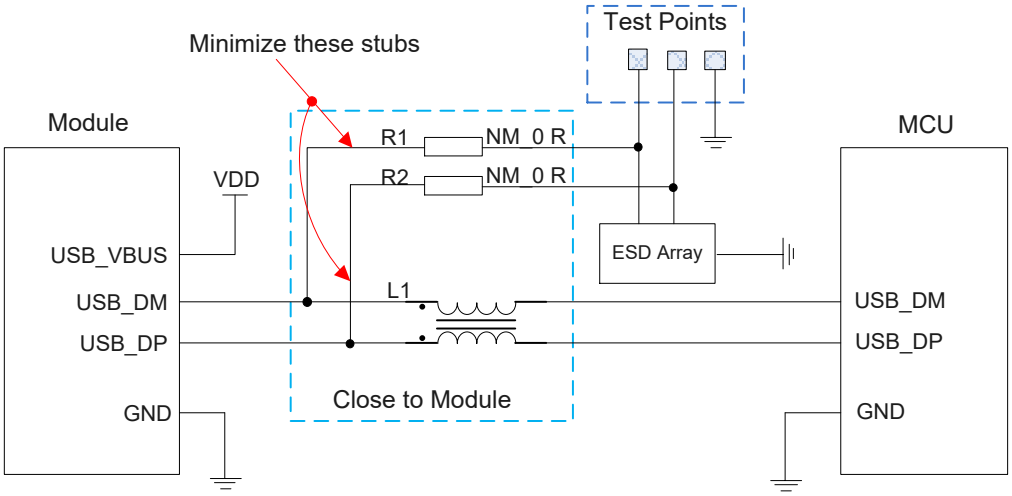


Figure 18: Reference Design of USB Interface

It is recommended to add a common-mode choke L1 in series between MCU and the module to suppress EMI. Meanwhile, it is also suggested to add R1 and R2 in series between the module and test points for debugging. These resistors are not mounted by default. To ensure the signal integrity of USB 2.0 data transmission, you should place L1, R1 and R2 close to the module, and keep these resistors close to each other. Moreover, keep extra stubs of trace as short as possible.

To ensure performance, you should follow the following principles when designing USB interface:

- Route USB signal traces as differential pairs with surrounded ground. The impedance of USB 2.0 differential trace is 90 Ω.
- Route USB differential traces at the inner-layer of the PCB, and surround the traces with ground on that layer and ground planes above and below. For signal traces, provide clearance from power supply traces, crystal-oscillators, magnetic devices, sensitive signals like RF signals, analog signals, and noise signals generated by clock, DC-DC, etc.
- Pay attention to the impact caused by stray capacitance of the ESD protection components on USB data traces. Typically, the stray capacitance should be less than 2 pF for USB 2.0 and the components should be placed close to the USB interface.

For more details about the USB specifications, visit http://www.usb.org/home.

4.2. Forced Download Interface

USB_BOOT is a forced download interface. Pull USB_BOOT down to GND before turning on the module, and then the module will enter forced download mode when it is turned on. In this mode, the module supports firmware upgrade over USB 2.0 interface.

Table 12: Pin Definition of Forced Download Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	115	DI	Force the module into forced download mode	1.8 V voltage domain. Active low. If the forced download function is not used, do not pull it to low level or high level and keep it open before the module is successfully turned on. A test point is recommended to be reserved.

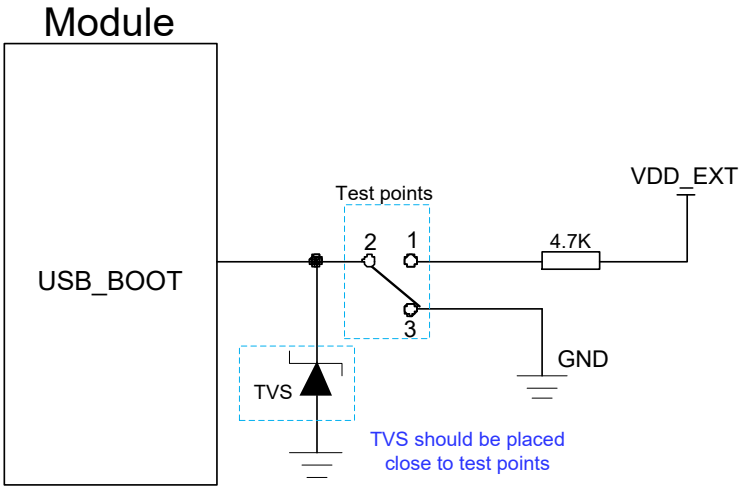


Figure 19: Reference Design of Forced Download Interface

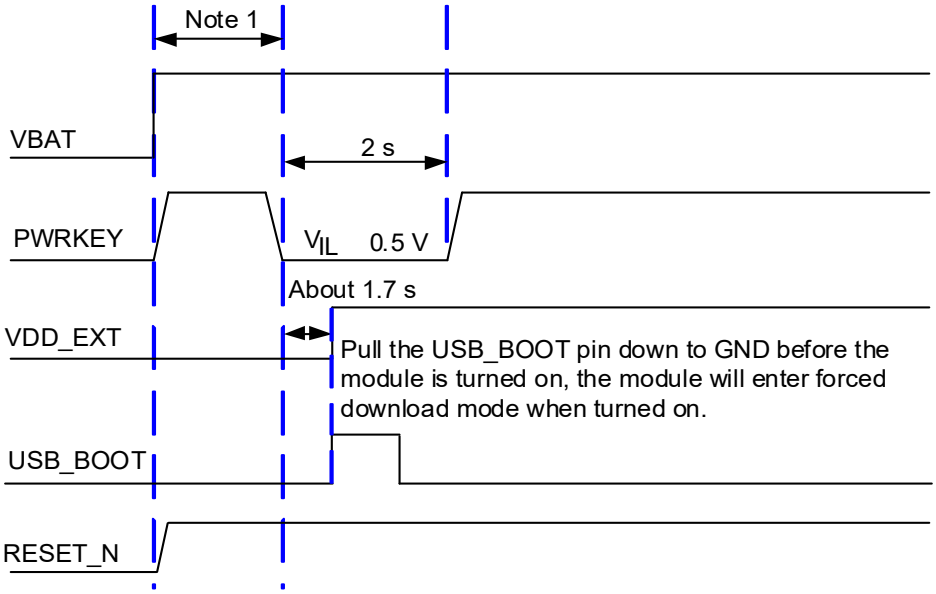


Figure 20: Timing of Entering Forced Download Mode

NOTE

1. Ensure VBAT is stable before driving PWRKEY low. The time period between powering VBAT up and driving PWRKEY low should be at least 30 ms.
2. Follow the above timing when MCU is used to control the module to enter the forced download mode. Do not pull up USB_BOOT to 1.8 V before powering on VBAT.
3. If you need to manually force the module to enter forced download mode, directly connect the test points shown in ***Figure 19***.
4. Considering the compatible design of EC200G-CN and EC200U series modules, the pull-up/down circuit design should be reserved.
   - Short-circuit test points 2 and 3 to set EC200G-CN into forced download mode.
   - Short-circuit test points 1 and 2 to set EC200U series into forced download mode.

4.3. USIM Interfaces [7]

The USIM interfaces meet ETSI and IMT-2000 requirements. Either 1.8 V or 3.0 V USIM card is supported.

[7] The USIM2 interface of the module is optional. If the hardware supports USIM2 interface, Dual SIM Dual Standby or Dual SIM Single Standby can be enabled through software configuration. For more details, contact Quectel Technical Support.

Table 13: Pin Definition of USIM1 Interface

Pin Name	Pin No.	I/O	Description	Comment
USIM1_VDD	14	PO	USIM1 card power supply	Either 1.8 V or 3.0 V USIM card is supported and can be identified automatically by the module.
USIM_GND	10	-	Specified ground for USIM card	Connect to the ground of USIM card connector.
USIM1_DATA	15	DIO	USIM1 card data	
USIM1_CLK	16	DO	USIM1 card clock	
USIM1_RST	17	DO	USIM1 card reset	
USIM1_DET	13	DI	USIM1 card hot-plug detect	1.8 V power domain. If unused, keep it open.

Table 14: Pin Definition of USIM2 Interface

Pin Name	Pin No.	USIM2 Function	I/O	Description	Comment
USIM2_VDD	128	-	PO	USIM2 card power supply	Either 1.8 V or 3.0 V USIM card is supported and can be identified automatically by the module.
AP_READY	2	USIM2_DATA	DIO	USIM2 card data	The USIM2 interface of the module is optional. You can use AP_READY, WAKEUP_IN, SLEEP_IND and W_DISABLE# to realize (U)SIM2 function in hardware design. Contact Quectel Technical Support for more details.
WAKEUP_IN	1	USIM2_CLK	DO	USIM2 card clock	
W_DISABLE#	4	USIM2_RST	DO	USIM2 card reset	
SLEEP_IND	3	USIM2_DET	DI	USIM2 card hot-plug detect	

The module supports USIM card hot-plug via the USIM_DET, and both high-level and low-level detections are supported. Hot-plug function is disabled by default, and you can use **AT+QSIMDET** to configure this function. See ***document [2]*** for more details about the **AT+QSIMDET**. The reference circuit of the 8-pin USIM interface is as follows.

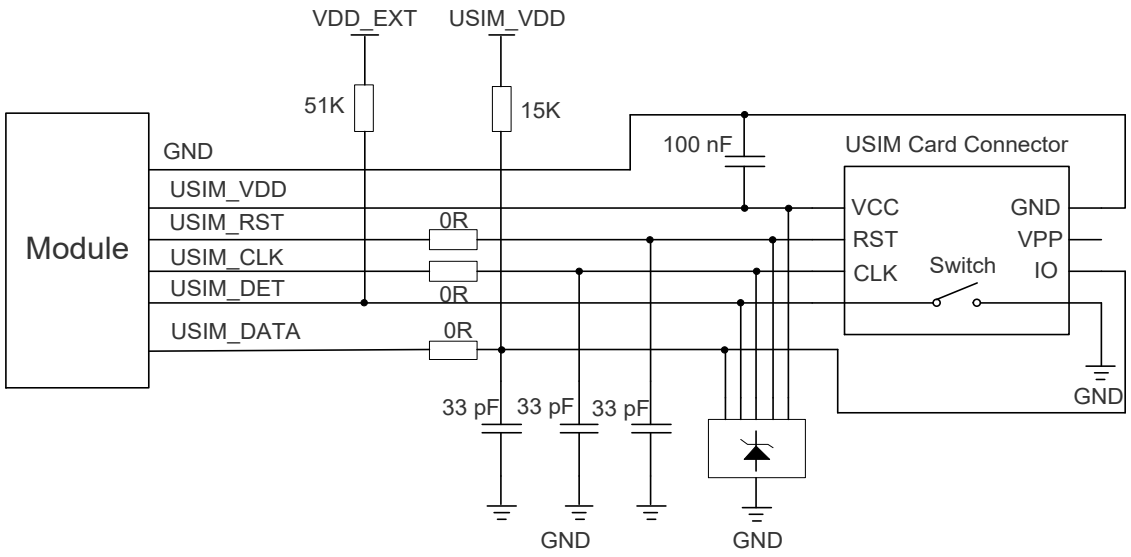


Figure 21: Reference Design of USIM Interface with an 8-pin USIM Card Connector

If the function of USIM card hot-plug is not needed, keep USIM_DET unconnected. The reference circuit of the 6-pin USIM interface is as follows.

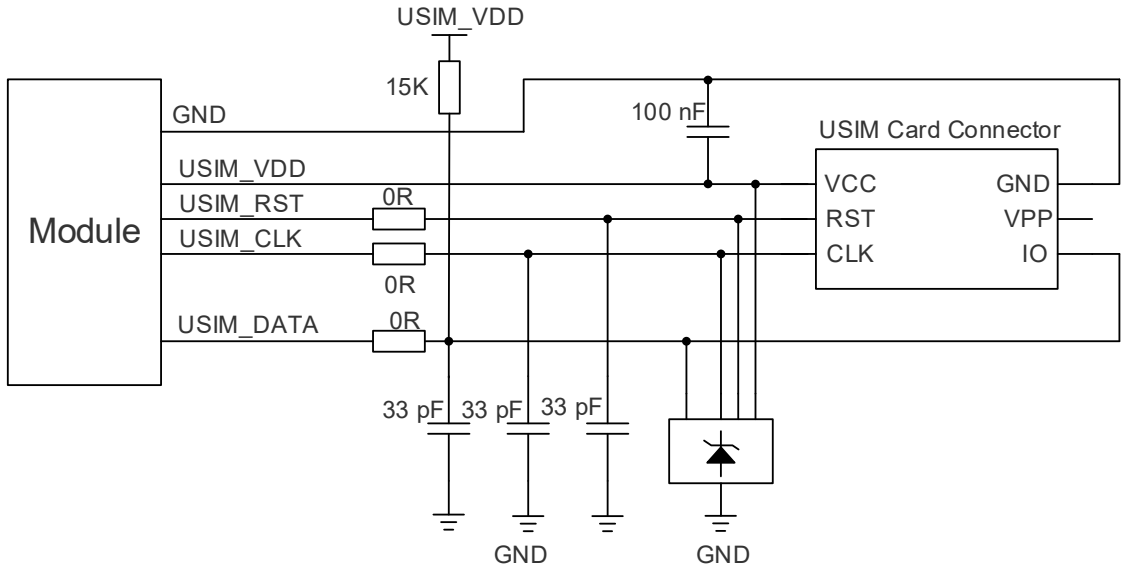


Figure 22: Reference Design of USIM Interface with a 6-pin USIM Card Connector

To enhance the reliability and availability of the USIM card in applications, you should follow the principles below in the USIM circuit design:

- Place the USIM card connector close to the module. Keep the trace length as short as possible, at most 200 mm.
- Keep USIM card signals away from RF and power supply traces.

- Ensure the bypass capacitor between USIM_VDD and GND is less than 1 μF, and the capacitor should be placed close to the USIM card connector.
- The GND of the USIM card connector should be connected directly to USIM_GND of the module. Keep the trace width of ground and USIM_VDD at least 0.5 mm to keep the same electric potential.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep the traces away from each other and shield them with surrounded ground.
- To offer better ESD protection, add a TVS array of which the parasitic capacitance should be less than 15 pF. Add 0 Ω resistors in series between the module and the USIM card connector to facilitate debugging. Additionally, add 33 pF capacitors in parallel among USIM_DATA, USIM_CLK and USIM_RST signal traces to filter out RF interference. Keep the (U)SIM peripheral circuit close to the (U)SIM card connector.
- For USIM_DATA, it is recommended to add a pull-up resistor near the USIM card connector to improve the anti-jamming capability of the USIM card.

4.4. UART

The module provides three UART: main UART, debug UART and auxiliary UART. The following table shows the UART information. For details on the baud rates supported by the UARTs, see ***document [2]***.

Table 15: UART Information

UART Type	Default Baud Rate	Function
Main UART	115200 bps	Data transmission and AT command communication; Supports RTS and CTS hardware flow control
Debug UART	2 Mbps	AP log output
Auxiliary UART	115200 bps	Data transmission

Table 16: Pin Definition of UART

Pin Name	Pin No.	I/O	Description	Comment
MAIN_CTS	64	DO	Clear to send signal from the module	Connect to MCU's CTS. 1.8 V power domain. If unused, keep it open.
MAIN_RTS	65	DI	Request to send signal to the module	Connect to MCU's RTS. 1.8 V power domain. If unused, keep it open.
MAIN_RXD	68	DI	Main UART receive	1.8 V power domain.

MAIN_DCD	63	DO	Main UART data carrier detection	If unused, keep them open.
MAIN_TXD	67	DO	Main UART transmit	
MAIN_RI	62	DO	Main UART ring indication	
MAIN_DTR	66	DI	Main UART data terminal ready	
AUX_TXD	138	DO	Auxiliary UART transmit	
AUX_RXD	137	DI	Auxiliary UART receive	
DBG_RXD	11	DI	Debug UART receive	1.8 V power domain. Test points must be reserved.
DBG_TXD	12	DO	Debug UART transmit	

The module provides a 1.8 V UART interface. You can use a voltage-level translator between the module and MCU's UART if the MCU is equipped with a 3.3 V UART.

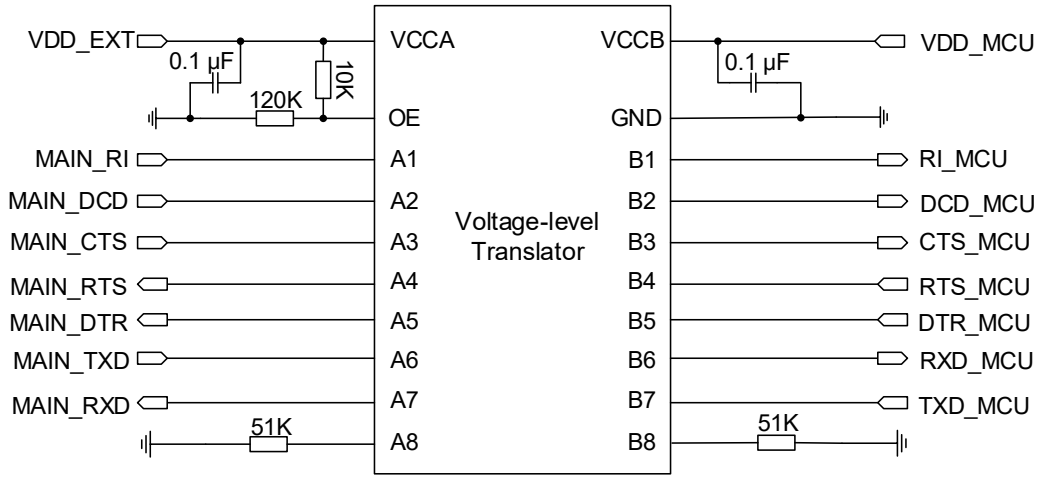


Figure 23: Reference Design of UART with a Voltage-level Translator (Main UART)

Another example of transistor circuit is shown as below. For the design of circuits in dotted lines, see that shown in solid lines, but pay attention to the direction of connection.

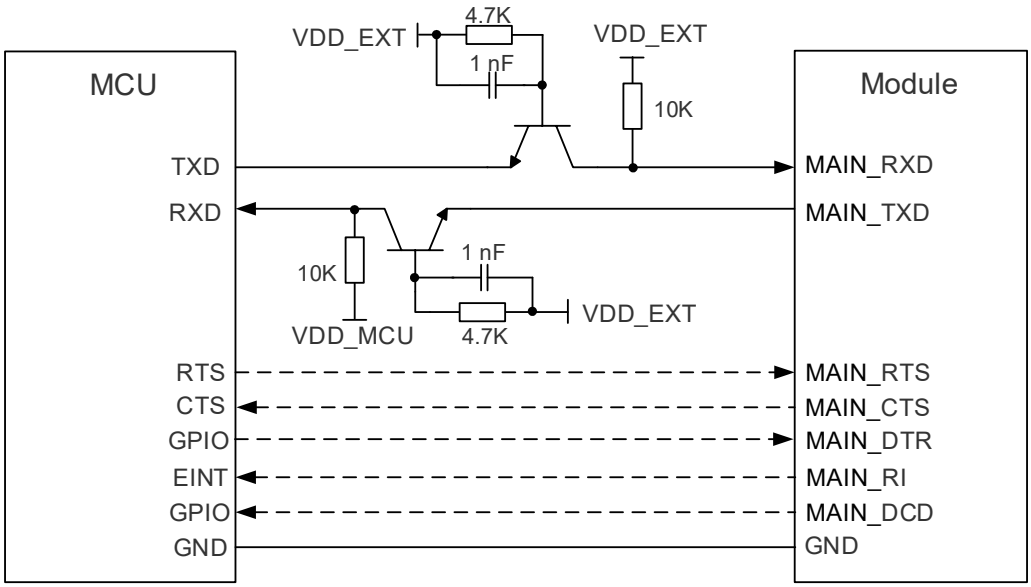


Figure 24: Reference Design of UART with Transistor Circuit (Main UART)

NOTE

1. Transistor circuit above is not suitable for applications with baud rates exceeding 460 kbps.
2. Please note that the module's CTS is connected to the MCU's CTS, and the module's RTS is connected to the MCU's RTS.
3. To increase the stability of UART communication, it is recommended to add UART hardware flow control design.

4.5. Analog Audio Interfaces (Optional)

The module provides one analog audio output channel and one analog audio input channel.

Table 17: Pin Definition of Analog Audio Interfaces

Pin Name	Pin No.	I/O	Description
SPK_P	73	AO	Analog audio differential output (+)
SPK_N	74	AO	Analog audio differential output (-)
MIC_P	75	AI	Microphone analog input (+)
MIC_N	77	AI	Microphone analog input (-)

- The audio output channel is a differential channel and can be applied for the earpiece output.
- The audio input channel is a differential channel and can be applied for the input of microphone (usually an electret microphone).

NOTE

1. If the limited output power of SPK channels does not meet your needs, install an external audio power amplifier.
2. There are pin conflicts among PCM interface, analog audio interface and PWM audio interface functions, and choose one of the three functions for implementing the audio function.

4.5.1. Audio Electrical Characteristics

Table 18: Analog Audio Interface Characteristics

Parameter		Min.	Typ.	Max.	Unit
Differential output	Load	16	32	-	Ω
	Common mode voltage	-	1.7	-	V
	Differential voltage	-	-	2.8	V_{pp}
	Output power	-	30	50	mW
Differential input	Differential voltage	-	-	2.6	V_{pp}

4.5.2. Audio Interface Design Considerations

It is recommended to use the electret microphone with dual built-in capacitors (e.g., 10 pF and 33 pF) to filter out RF interference, thus reducing TDD noise. Note that the resonant frequency point of a capacitor largely depends on the material and production technique. Therefore, you need to discuss with your capacitor vendors to choose the most suitable capacitor to filter out high-frequency noises.

The filter capacitor on the PCB should be placed near the audio device or audio interface as close as possible, and the trace should be as short as possible. The filter capacitor should be passed before reaching other connection points.

To decrease signal interferences, RF antennas should be placed away from audio interfaces and audio traces. Power traces and audio traces should not be parallel, and they should be far away from each other.

The differential audio traces must be routed according to the differential signal layout rule.

4.5.3. Microphone Interface Circuit

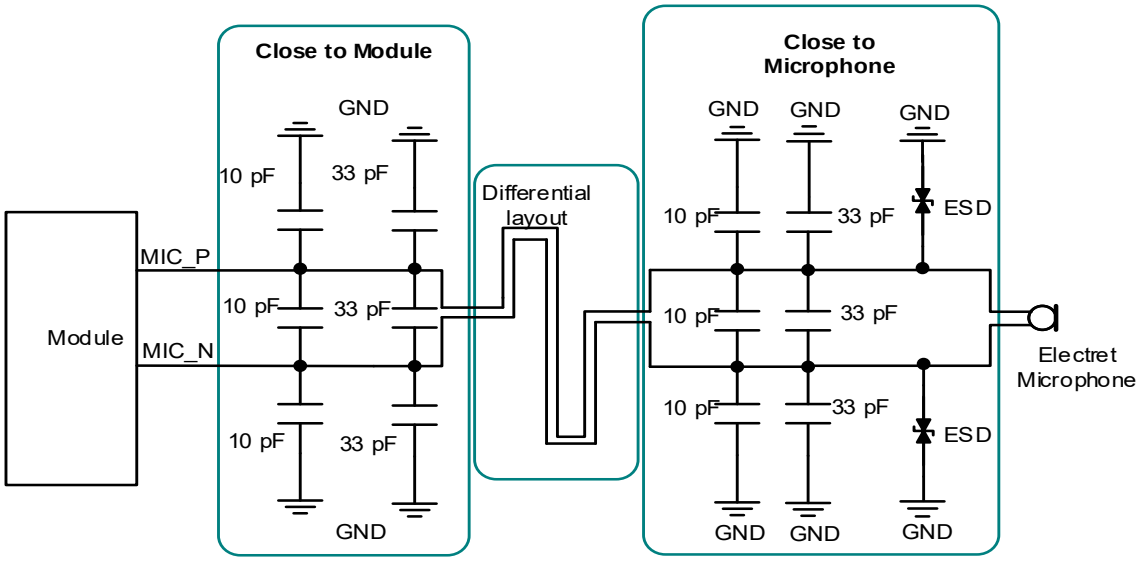


Figure 25: Reference Circuit of Microphone Interface

NOTE

Microphone channel is sensitive to ESD, so it is not recommended to remove ESD protection components.

4.5.4. Earpiece Interface Circuit

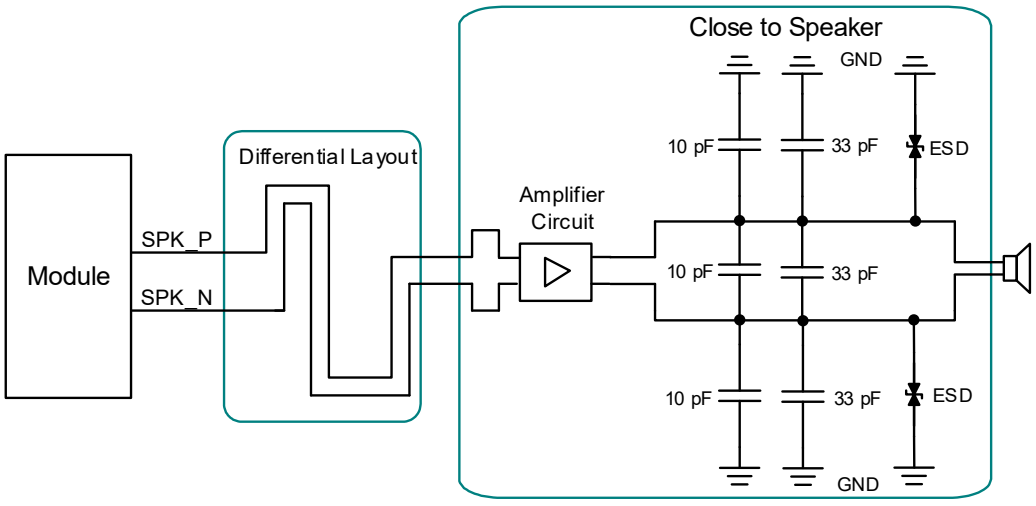


Figure 26: Reference Design of Earpiece Interface with External PA

4.6. PCM (Optional) and I2C Interfaces

The module provides one PCM interface supporting master mode and two I2C interfaces. The PCM interface can be used for connecting the external audio codec chip.

Table 19: Pin Definition of PCM Interface

Pin Name	Pin No.	I/O	Description	Comment
PCM_DIN	24	DI	PCM data input	1.8 V power domain. If unused, keep them open.
PCM_DOUT	25	DO	PCM data output	
PCM_SYNC	26	DO	PCM data frame sync	
PCM_CLK	27	DO	PCM clock	

Table 20: Pin Definition of I2C Interfaces

Pin Name	Pin No.	I/O	Description	Comment
I2C1_SCL	41	OD	I2C1 serial clock	1.8 V power domain. An external 1.8 V pull-up resistor is needed. If unused, keep them open.
I2C1_SDA	42	OD	I2C1 serial data	
I2C2_SCL	141	OD	I2C2 serial clock	
I2C2_SDA	142	OD	I2C2 serial data	

The following figure shows the reference design of PCM and I2C interfaces with an external codec chip:

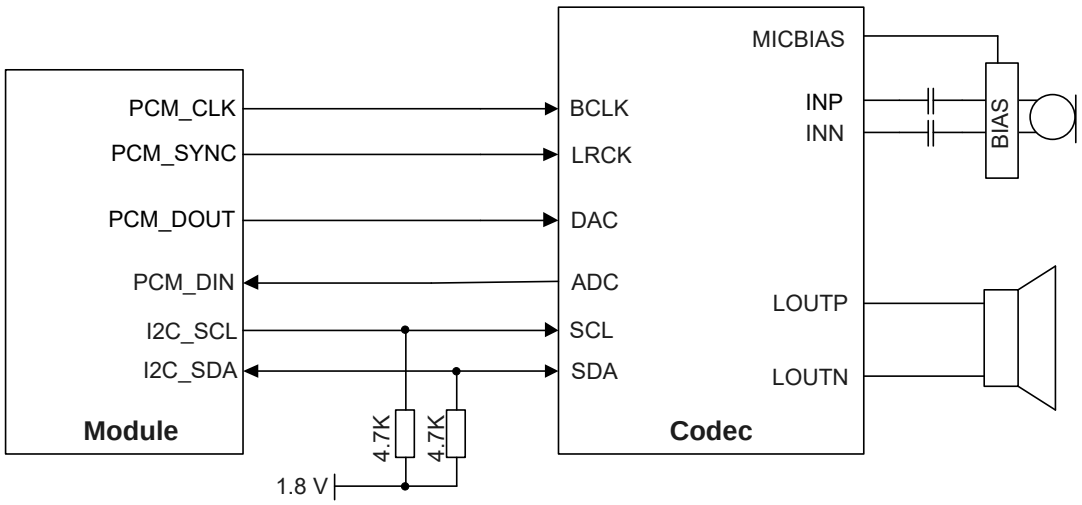


Figure 27: Reference Design of PCM and I2C Interfaces

NOTE

1. It is recommended to reserve an RC (R = 0 Ω, C = 33 pF) circuit on the PCM traces, especially on PCM_CLK.
2. There are pin conflicts among PCM interface, analog audio interface and PWM audio interface functions, and choose one of the three functions for implementing the audio function.
3. The I2C interfaces support simultaneous connection of multiple peripherals except for codec IC. In other words, if a codec IC has been mounted on the I2C bus, no other peripherals can be mounted; if there is no codec IC on the bus, multiple peripherals can be mounted.
4. The module can only be used as a master device in applications related to PCM and I2C interfaces.

4.7. PWM Audio Interface (Optional)

The module supports PWM playback of audio files/streams (recording is not supported), and supports 8–44.1 kHz sampling rate. If the requirements for sound quality are not very high, PWM channels can be used to playback audio.

Table 21: Pin Definition of PWM Audio Interface

Pin Name	Pin No.	PWM Function	I/O	Description	Comment
PCM_DIN	24	PA_EN	DO	PA enable	1.8 V power domain. If unused, keep them open.
PCM_DOUT	25	PWM_AUDIO	DO	PWM audio output	

The reference design is as follows:

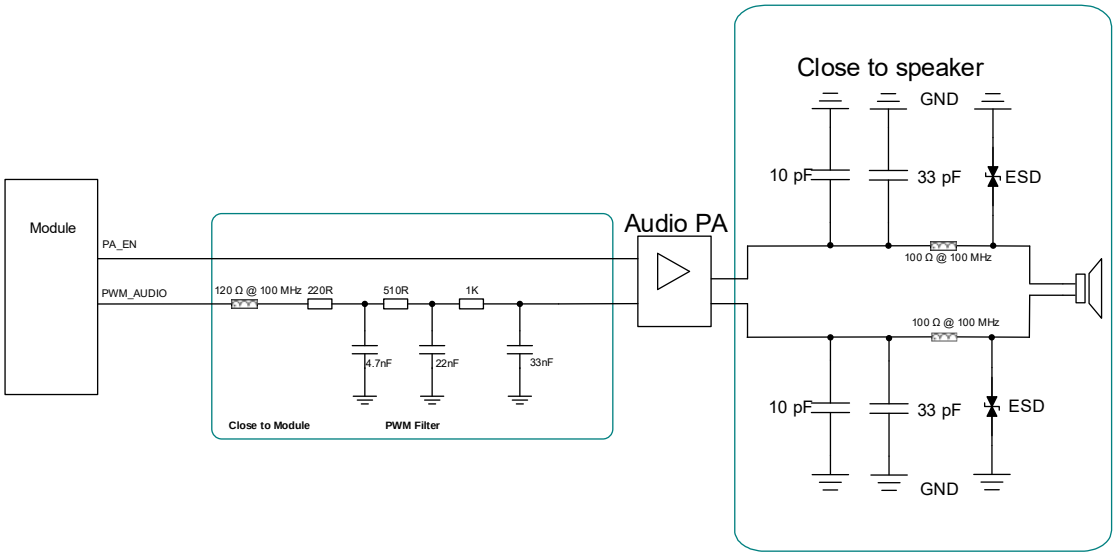


Figure 28: PWM Audio Interface Circuit Reference Design

NOTE

1. There are pin conflicts among PCM interface, analog audio interface and PWM audio interface functions, and choose one of the three functions for implementing audio function. Contact Quectel Technical Support for details.
2. You can switch between PCM, analog audio and PWM audio functions via **AT+QAUDSW**. See ***document [4]*** for details.

4.8. ADC Interfaces

The module provides three ADC interfaces. To improve the measurement accuracy of ADC, the traces of ADC interfaces should be surrounded by ground.

Table 22: Pin Definition of ADC Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ADC0	45	AI	General-purpose ADC interface	Use a 1 kΩ resistor in series. If a voltage divider resistor is used, the external voltage divider resistor must be less than 100 kΩ. If unused, keep them open.
ADC1	44	AI		
ADC2	43	AI		

With **AT+QADC=<port>**, you can:

- **AT+QADC=0**: read the voltage value on ADC0
- **AT+QADC=1**: read the voltage value on ADC1
- **AT+QADC=2**: read the voltage value on ADC2

For more details about the AT command, see ***document [2]***.

Table 23: Characteristics of ADC Interfaces

Parameter	Min.	Typ.	Max.	Unit
ADC[0:2] input voltage range	0	-	VBAT	V
ADC resolution	-	11	-	bits

NOTE

1. The input voltage of each ADC interface should not exceed its corresponding voltage range.
2. It is prohibited to directly supply any voltage to ADC interfaces when the module is not powered by the VBAT.
3. Considering the possible difference of ADC voltage range among Quectel modules, when using ADC pins, it is strongly recommended to reserve a voltage divider circuit for better compatibility with other Quectel modules. The resistance of the voltage divider resistor must be less than 100 kΩ, otherwise the measurement accuracy of the ADC will be significantly reduced. When the divider circuit is not used, the ADC pins require 1 kΩ resistors in series.

4.9. Indication Signals

Table 24: Pin Definition of Indication Signals

Pin Name	Pin No.	I/O	Description	Comment
NET_MODE	5	DO	Indicate the module's network registration mode	1.8 V power domain. If unused, keep them open.
NET_STATUS	6	DO	Indicate the module's network activity status	
STATUS	61	DO	Indicate the module's operation status	
MAIN_RI	62	DO	Main UART ring indication	

4.9.1. Network Status Indication

The module has two network status indication pins: the NET_MODE for the module's network registration mode indication and the NET_STATUS for the module's network activity indication. Both can drive corresponding LEDs.

Table 25: Network Status Indication Pin Level and Module Network Status

Pin Name	Level Status	Module Network Status
NET_MODE	Always high	Registered on LTE network
	Always low	Others
NET_STATUS	Blink slowly (200 ms high/1800 ms low)	Network searching
	Blink slowly (1800 ms high/200 ms low)	Idle
	Blink quickly (125 ms high/125 ms low)	Data transmission is ongoing

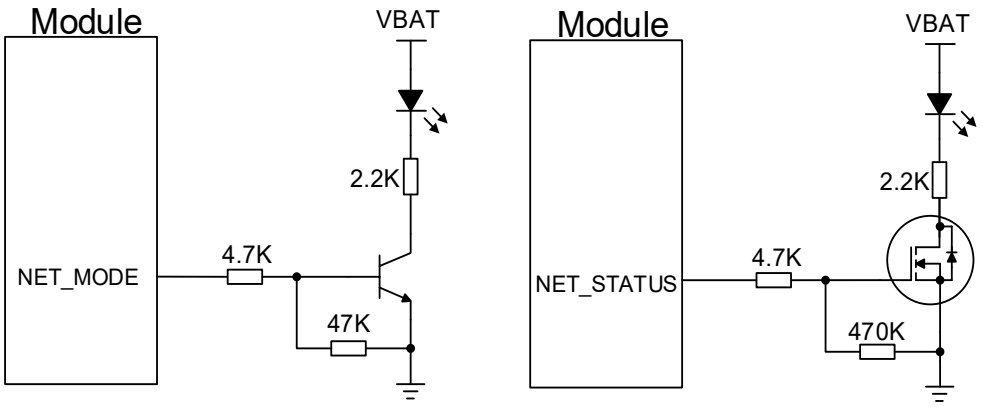


Figure 29: Reference Design of Network Status Indication

4.9.2. STATUS

The STATUS is used for indicating module's operation status. It will output high level when the module is turned on normally.

A reference circuit is shown in the following figure.

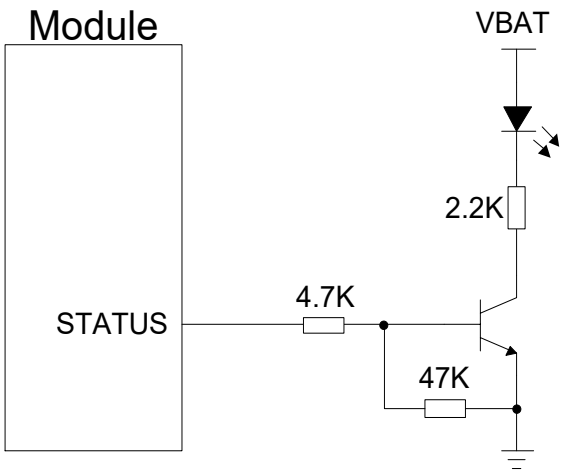


Figure 30: Reference Design of STATUS

4.9.3. MAIN_RI

AT+QCFG="risignaltype","physical" can be used to configure the indication behavior for MAIN_RI. No matter on which port (main UART, USB AT port or USB modem port) a URC information is presented, the URC information will trigger the behavior of the MAIN_RI. For more details, see ***document [2]***.

NOTE

The **AT+QURCCFG** allows you to set the main UART, USB AT port or USB modem port as the URC output port. The USB AT port is the URC output port by default. For more details, see ***document [2]***.

You can configure MAIN_RI behaviors flexibly. The default behaviors of the MAIN_RI is shown as below:

Table 26: MAIN_RI Behaviors

State	Response
Idle	High
When a new URC returns	MAIN_RI outputs at least 120 ms low level. After the module outputs the data, the level status will then become high.

Indication behavior for MAIN_RI can be configured via **AT+QCFG="urc/ri/other"**. See ***document [2]*** for details.

5 RF Specifications

Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to perform a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

5.1. LTE/Wi-Fi Scan Antenna Interface

5.1.1. RF Antenna Interface & Frequency Bands

Table 27: Pin Definition of RF Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN/WIFI_SCAN [8]	49	AIO/ AI	LTE/Wi-Fi Scan antenna interface	50 Ω characteristic impedance.

Table 28: Operating Frequency (Unit: MHz)

Operating Frequency	Transmit	Receive
LTE-FDD B1	1920–1980	2110–2170
LTE-FDD B3	1710–1785	1805–1880
LTE-FDD B5	824–849	869–894
LTE-FDD B8	880–915	925–960
LTE-TDD B34	2010–2025	2010–2025
LTE-TDD B38	2570–2620	2570–2620
LTE-TDD B39	1880–1920	1880–1920

[8] Wi-Fi Scan shares the same antenna interface with the main antenna. The two functions cannot be used at the same time, and Wi-Fi Scan only supports receiving.

LTE-TDD B40	2300–2400	2300–2400
LTE-TDD B41	2535–2675	2535–2675

5.1.2. Tx Power

Table 29: RF Transmitting Power

Frequency Band	Max.	Min.
LTE-FDD B1/B3/B5/B8	23 dBm ±2 dB	< -39 dBm
LTE-TDD B34/B38/B39/B40/B41	23 dBm ±2 dB	< -39 dBm

5.1.3. Rx Sensitivity

Table 30: Conducted RF Receiver Sensitivity (Unit: dBm)

Frequency	Receiver Sensitivity (Typ.)	3GPP Requirement
	Primary	
LTE-FDD B1 (10 MHz)	-98.0	-96.3
LTE-FDD B3 (10 MHz)	-97.0	-93.3
LTE-FDD B5 (10 MHz)	-97.5	-94.3
LTE-FDD B8 (10 MHz)	-98.0	-93.3
LTE-TDD B34 (10 MHz)	-99.0	-96.3
LTE-TDD B38 (10 MHz)	-99.0	-96.3
LTE-TDD B39 (10 MHz)	-99.5	-96.3
LTE-TDD B40 (10 MHz)	-99.5	-96.3
LTE-TDD B41 (10 MHz)	-98.5	-94.3

NOTE

The RF receiver sensitivity data of EC200G-CN above is for reference only. For more details, contact Quectel Technical Support.

5.1.4. Reference Design

The module provides one RF antenna interface. A π-type matching circuit should be reserved for better RF performance. The capacitors are not mounted by default. C1, R1, and C2 should be placed as close to the antenna as possible.

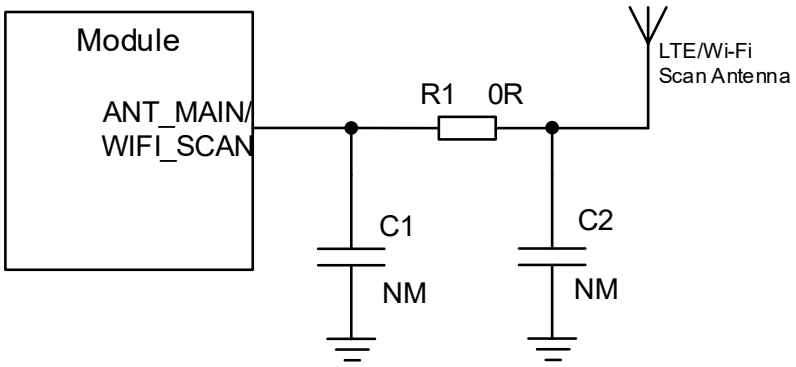


Figure 31: Reference Design of LTE/Wi-Fi Scan Antenna

5.2. Bluetooth Antenna Interface (Optional)

5.2.1. Antenna Interface

Table 31: Pin Definition of Bluetooth Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_BT	35	AIO	Bluetooth antenna interface	50 Ω characteristic impedance. If unused, keep it open.

5.2.2. Reference Design

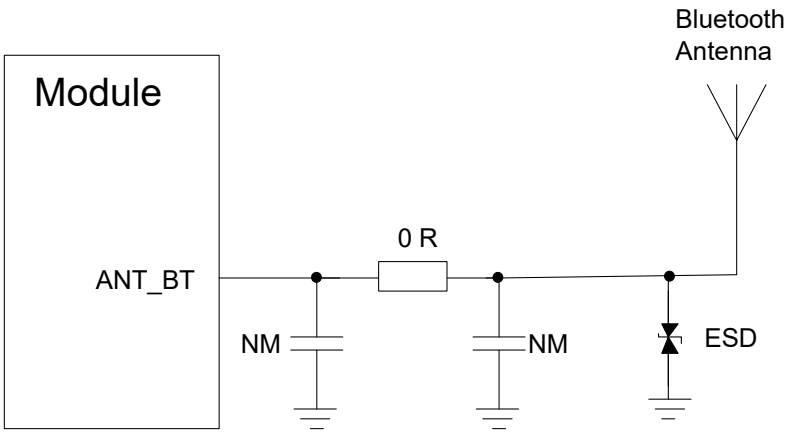


Figure 32: Reference Design of Bluetooth Interface

5.3. GNSS (Optional)

GNSS information of the module is as follows:

- Supports GPS, BDS, QZSS positioning system.
- Supports NMEA 0183 protocol and outputs NMEA sentences via USB interface by default.
- The module's GNSS function is OFF by default. It must be enabled via **AT+QGPS**. For more details, see ***document [5]***.

5.3.1. Antenna Interface & Frequency Bands

Table 32: Pin Definition of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	47	AI	GNSS antenna interface	50 Ω characteristic impedance. If unused, keep it open.

Table 33: Frequency (Unit: MHz)

Antenna Type	Frequency
GPS	1575.42 ±1.023
BDS	1561.098 ±2.046
QZSS	1575.42 ±1.023

5.3.2. GNSS Performance

Table 34: GNSS Performance

Parameter	Mode	Condition	Typ.	Unit
Sensitivity	Acquisition	Autonomous	-164	dBm
	Reacquisition		-159	
	Tracking		-148	
TTFF	Cold start @ open sky	Autonomous	28.02	s
	Warm start @ open sky		27.95	
	Hot start @ open sky		0.47	
Accuracy	CEP-50	Autonomous @ open sky	0.92	m

NOTE

1. Tracking sensitivity: the minimum GNSS signal power at which the module can maintain lock (keep positioning for at least 3 minutes continuously).
2. Reacquisition sensitivity: the minimum GNSS signal power required for the module to maintain lock within 3 minutes after loss of lock.
3. Acquisition sensitivity: the minimum GNSS signal power at which the module can fix position successfully within 3 minutes after executing cold start command.

5.3.3. Reference Design

5.3.3.1. GNSS Active Antenna

GNSS active antenna connection reference circuit is shown in the figure below.

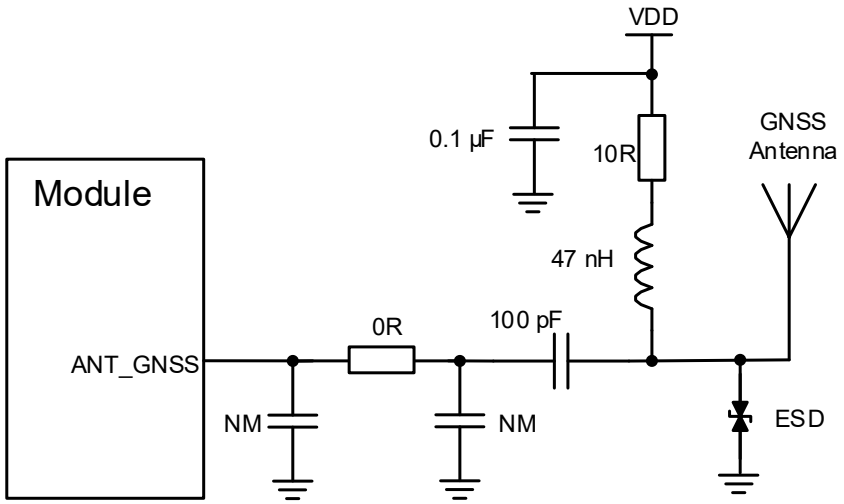


Figure 33: Reference Design of GNSS Active Antenna

The power supply voltage range of the external active antenna is 2.8–4.3 V, and the typical value is 3.3 V.

5.3.3.2. GNSS Passive Antenna

GNSS passive antenna connection reference circuit is shown in the figure below.

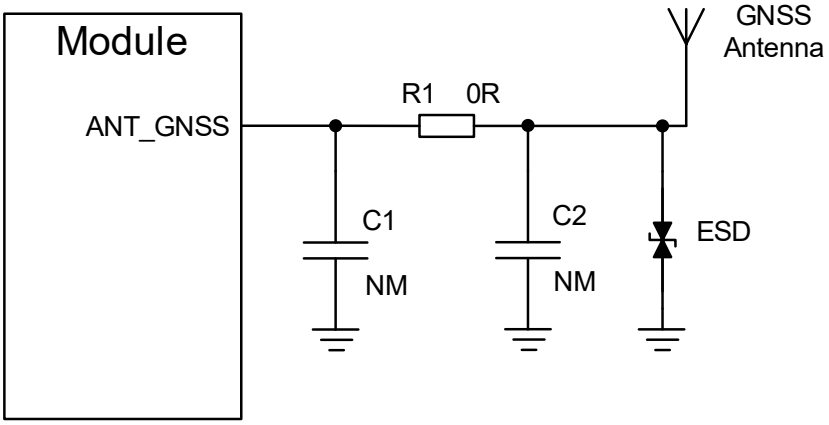


Figure 34: Reference Design of GNSS Passive Antenna

It is recommended to reserve a π-type matching circuit in the circuit design for antenna interface for better RF performance. Components (C1, R1 and C2) of the π-type matching circuit shall be placed as close to the antenna as possible. C1, C2 are not mounted by default. Only a 0 Ω resistor is mounted on R1. Keep the impedance for RF trace as 50 Ω when routing and keep the trace as short as possible.

NOTE

1. You can select an external LDO according to the active antenna types.
2. Junction capacitance of ESD protection components should not exceed 0.05 pF.
3. GNSS application design should follow the following design principles:
   - The distance between the GNSS antenna and the main antenna, Wi-Fi Scan antenna or Bluetooth antenna should be as large as possible, and the isolation should be at least 20 dB.
   - Digital signals such as USIM card, USB interface, camera module, SD card and display interface should be kept away from the antenna.
   - Sensitive analog signals should be kept away from the GNSS signal path, and GNSS holes should be added for isolation and protection.

5.4. RF Routing Guidelines

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

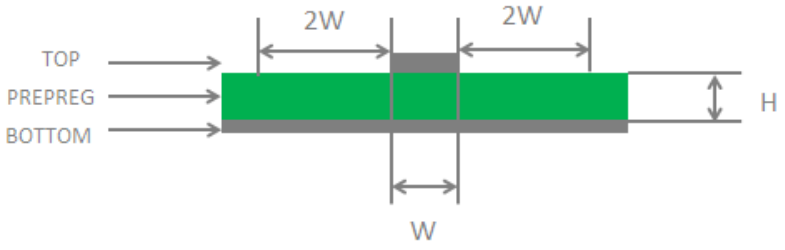


Figure 35: Microstrip Design on a 2-layer PCB

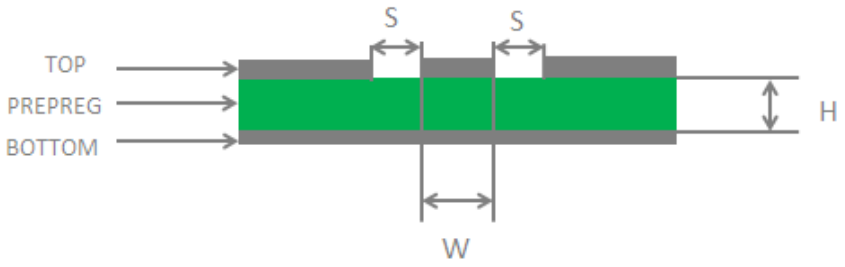


Figure 36: Coplanar Waveguide Design on a 2-layer PCB

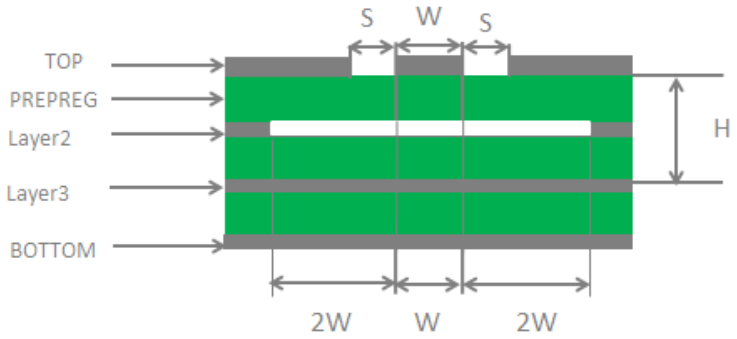


Figure 37: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

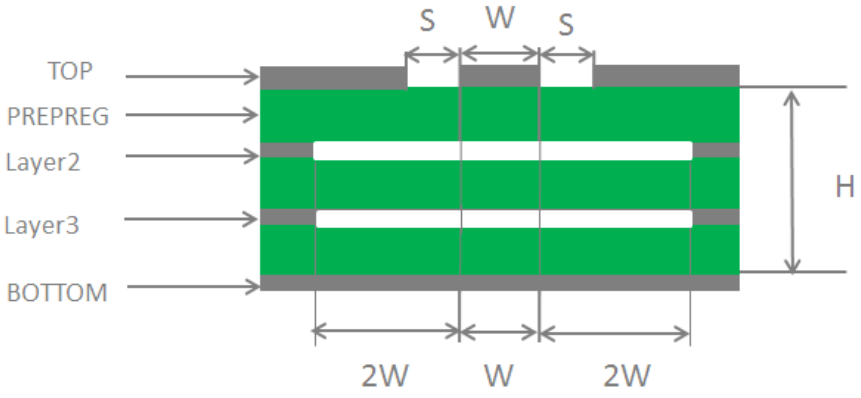


Figure 38: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.

- GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should not be less than twice the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between any traces on adjacent layers.

For more details about RF layout, see ***document [6]***.

5.5. Antenna Design Requirements

Table 35: Antenna Design Requirements

Antenna Type	Requirement
GNSS (Optional)	Frequency range: L1 (1559–1609 MHz) RHCP or linear polarization VSWR: ≤ 2 (Typ.)
	For passive antenna usage: Passive antenna gain: > 0 dBi
	For active antenna usage: Active antenna noise coefficient: < 1.5 dB Active antenna embedded LNA gain: < 23 dB
LTE/Wi-Fi Scan	VSWR: ≤ 2 Efficiency: > 30 % Gain: 1 dBi Max input power: 50 W Input impedance: 50 Ω Vertical polarization Cable insertion loss: ● **< 1 dB:** LB (< 1 GHz) ● **< 1.5 dB:** MB (1–2.3 GHz) ● **< 2 dB:** HB (> 2.3 GHz)

5.6. RF Connector Recommendation

If RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT receptacle provided by Hirose.

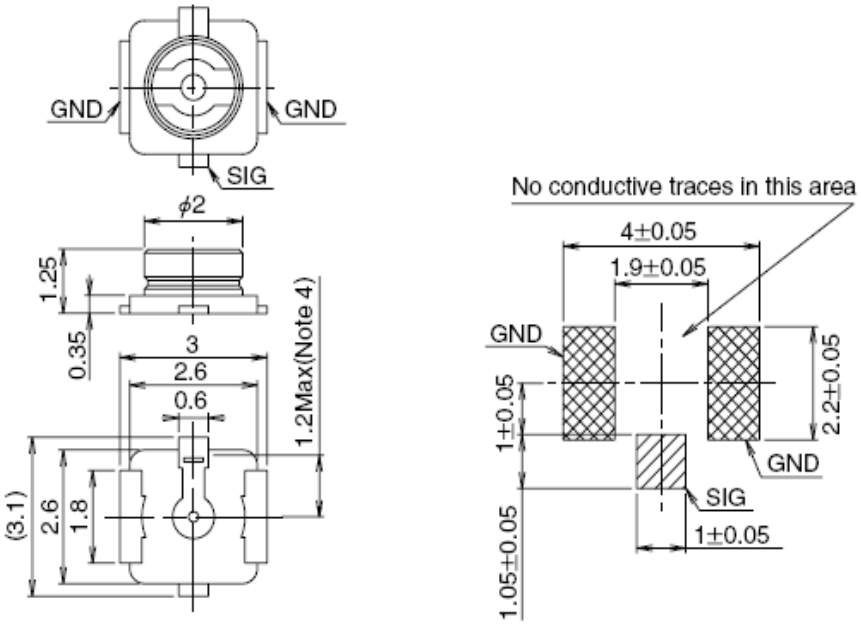


Figure 39: Dimensions of the Receptacle (Unit: mm)

U.FL-LP series mated plugs listed in the following figure can be used to match the U.FL-R-SMT.

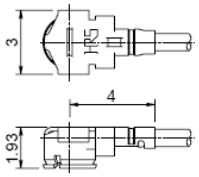
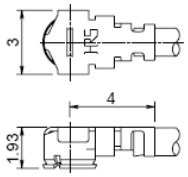
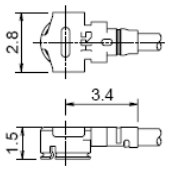
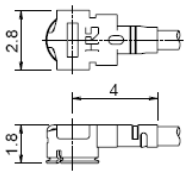
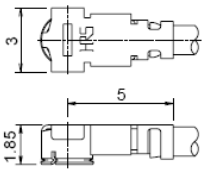
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 40: Specifications of Mated Plugs (Unit: mm)

The following figure describes the space factor of the mated connectors.

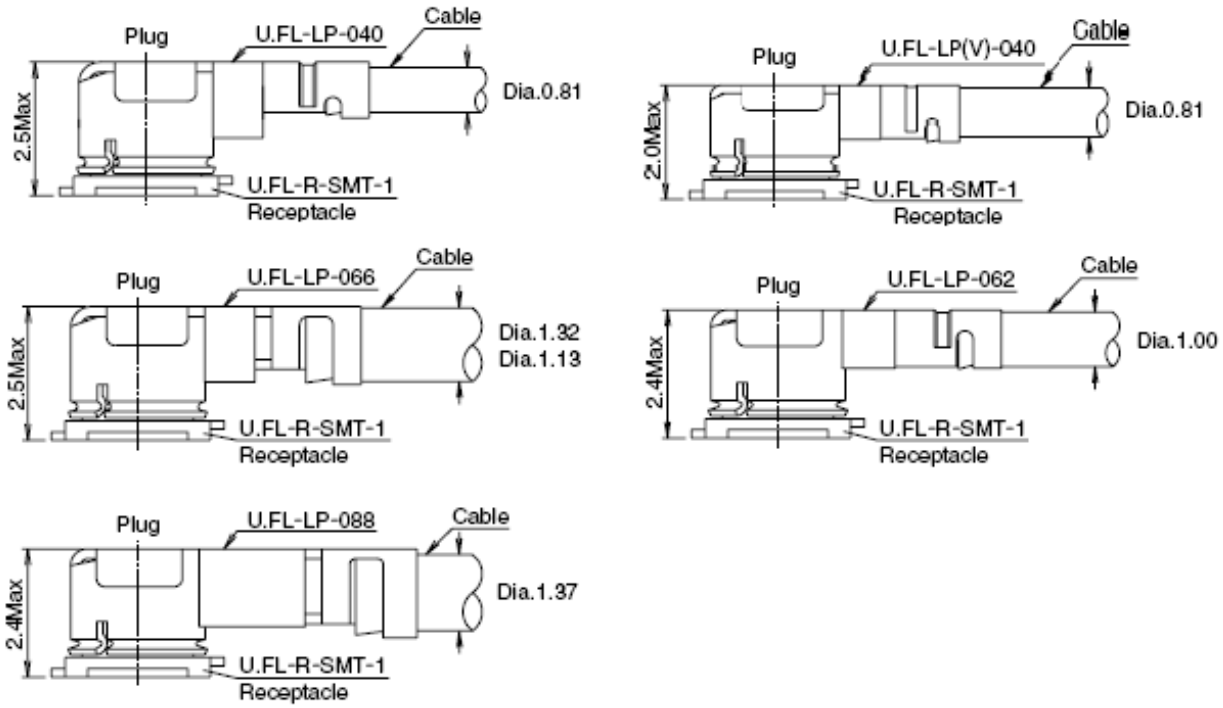


Figure 41: Space Factor of the Mated Connectors (Unit: mm)

For more details, visit http://www.hirose.com.

6 Electrical Characteristics and Reliability

6.1. Absolute Maximum Ratings

Table 36: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
Voltage at VBAT_BB & VBAT_RF	-0.3	6.0	V
Voltage at USB_VBUS	-0.3	5.5	
Voltage at digital pins	-0.3	2.3	
Input voltage at ADC[0:2]	0	VBAT	
Current at VBAT_BB & VBAT_RF	-	2.0	A

6.2. Power Supply Ratings

Table 37: Module's Power Supply Ratings

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF	The actual input voltage must be within this range	3.3	3.8	4.3	V
I_{VBAT}	Peak power consumption	At maximum power control level	-	-	2	A
USB_VBUS	USB connection detection		3.5	5.0	5.25	V

6.3. Power Consumption

Table 38: Power Consumption

Mode	Condition	Typ.	Unit
OFF state	Power off	8.49	μA
Sleep state	**AT+CFUN=0** (USB disconnected)	1.40	mA
	AT+CFUN=4 (USB disconnected)	1.49	
	LTE-FDD @ PF = 32 (USB disconnected)	3.27	
	LTE-FDD @ PF = 64 (USB disconnected)	1.82	
	LTE-FDD @ PF = 64 (USB suspended)	3.11	
	LTE-FDD @ PF = 128 (USB disconnected)	1.87	
	LTE-FDD @ PF = 256 (USB disconnected)	1.17	
	LTE-TDD @ PF = 32 (USB disconnected)	3.26	
	LTE-TDD @ PF = 64 (USB disconnected)	2.35	
	LTE-TDD @ PF = 64 (USB suspended)	3.12	
	LTE-TDD @ PF = 128 (USB disconnected)	1.87	
	LTE-TDD @ PF = 256 (USB disconnected)	1.66	
Idle state	LTE-FDD @ PF = 64 (USB disconnected)	16.58	mA
	LTE-FDD @ PF = 64 (USB connected)	29.53	
	LTE-TDD @ PF = 64 (USB disconnected)	16.61	
	LTE-TDD @ PF = 64 (USB connected)	29.53	
LTE data transmission	LTE-FDD B1 @ 23.42 dBm	680	mA
	LTE-FDD B3 @ 23.28 dBm	680	
	LTE-FDD B5 @ 23.24 dBm	530	
	LTE-FDD B8 @ 23.62 dBm	620	

	LTE-TDD B34 @ 22.89 dBm	258
	LTE-TDD B38 @ 23.34 dBm	265
	LTE-TDD B39 @ 23.02 dBm	235
	LTE-TDD B40 @ 22.98 dBm	250
	LTE-TDD B41 @ 23.17 dBm	280

6.4. Digital I/O Characteristics

Table 39: 1.8 V I/O Characteristics (Unit: V)

Parameter	Description	Min.	Max.
V_{IH}	High-level input voltage	0.7 × VDDIO	VDDIO + 0.2
V_{IL}	Low-level input voltage	0	0.3 × VDDIO
V_{OH}	High-level output voltage	0.9 × VDDIO	VDDIO
V_{OL}	Low-level output voltage	0	0.1 × VDDIO

NOTE

VDDIO is power domain of the module's I/O pins.

Table 40: USIM Low-voltage I/O Characteristics (Unit: V)

Parameter	Description	Min.	Max.
USIM_VDD	Power supply	1.62	1.98
V_{IH}	High-level input voltage	0.7 × USIM_VDD	USIM_VDD
V_{IL}	Low-level input voltage	0	0.2 × USIM_VDD
V_{OH}	High-level output voltage	0.7 × USIM_VDD	USIM_VDD
V_{OL}	Low-level output voltage	0	0.15 × USIM_VDD

Table 41: USIM High-voltage I/O Characteristics (Unit: V)

Parameter	Description	Min.	Max.
USIM_VDD	Power supply	2.7	3.3
V_{IH}	High-level input voltage	0.7 × USIM_VDD	USIM_VDD
V_{IL}	Low-level input voltage	0	0.15 × USIM_VDD
V_{OH}	High-level output voltage	0.7 × USIM_VDD	USIM_VDD
V_{OL}	Low-level output voltage	0	0.15 × USIM_VDD

6.5. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

Table 42: ESD Characteristics (Temperature: 25–30 °C, Humidity: 40 ±5 %)

Tested Interface	Contact Discharge	Air Discharge	Unit
VBAT & GND	±5	±10	kV
All antenna interfaces	±4	±8	
Other interfaces	±0.5	±1	

6.6. Operating and Storage Temperatures

Table 43: Operating and Storage Temperatures (Unit: °C)

Parameter	Min.	Typ.	Max.
Normal operating temperature [9]	-35	+25	+75
Extended operating temperature [10]	-40	-	+85
Storage temperature	-40	-	+90

[9] Within this range, the module's indicators comply with 3GPP specification requirements.

[10] Within this range, the module retains the ability to establish and maintain functions such as voice*, SMS, data transmission, and emergency call*, without any unrecoverable malfunction. Radio spectrum and radio network remain uninfluenced, whereas the value of one or more parameters, such as P_{out}, may decrease and fall below the range of the 3GPP specified tolerances. When the temperature returns to the normal operating temperature range, the module's performance will comply with 3GPP specification requirements again.

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

7.1. Mechanical Dimensions

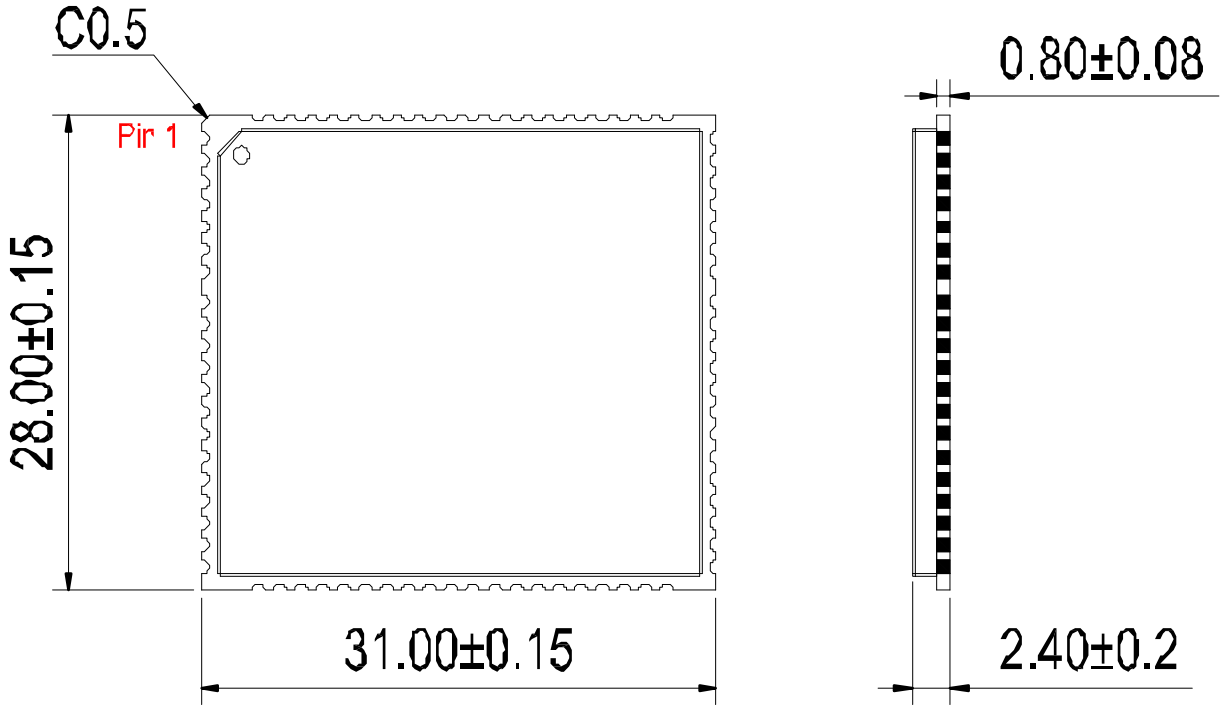


Figure 42: Top and Side Dimensions

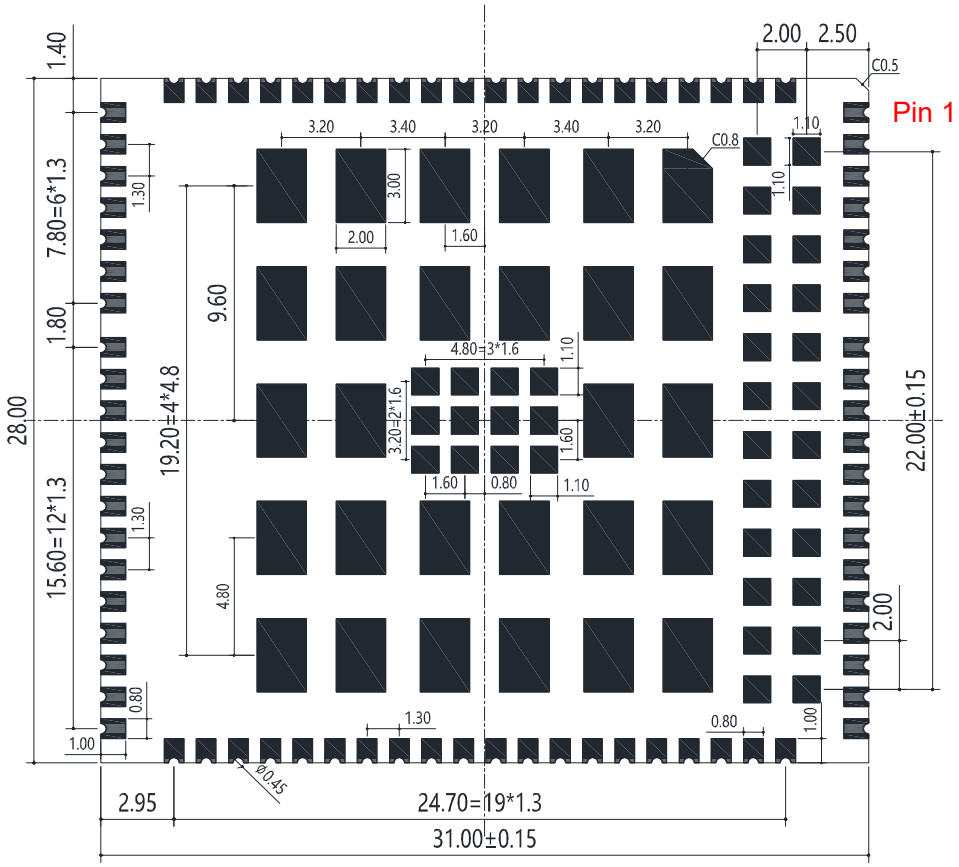


Figure 43: Bottom Dimensions

NOTE

The package warpage level of the module refers to the *JEITA ED-7306* standard.

7.2. Recommended Footprint

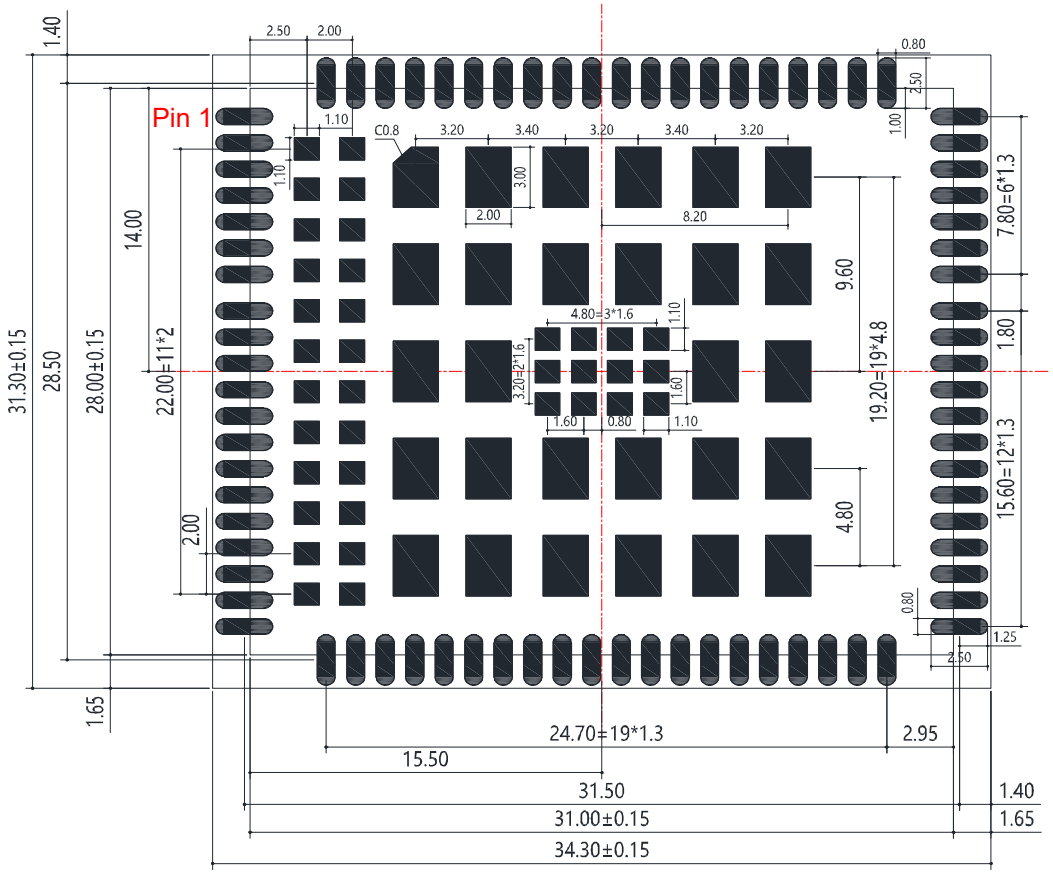


Figure 44: Recommended Footprint

NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

7.3. Top and Bottom Views

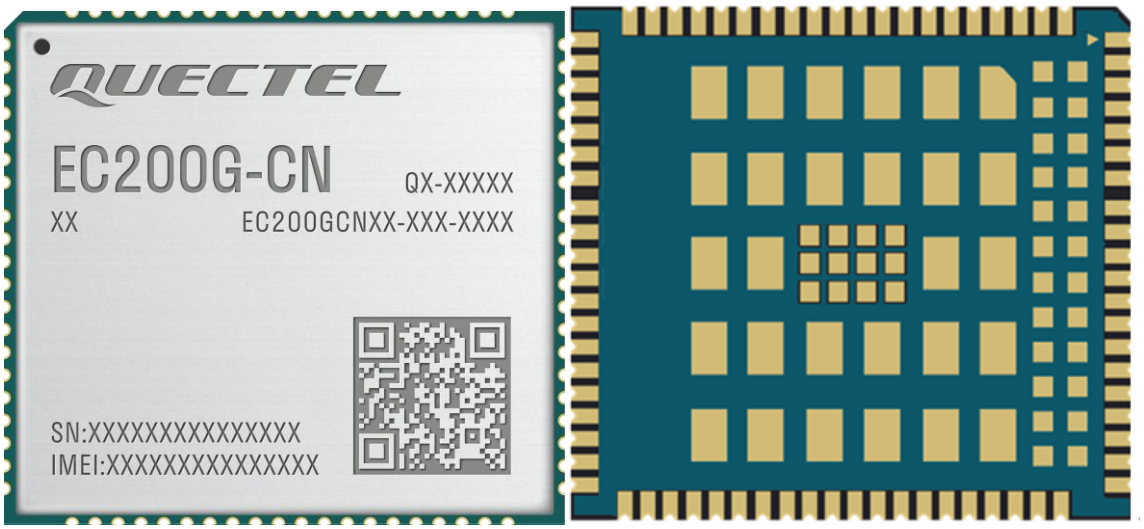


Figure 45: Top & Bottom Views of the Module

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

8 Storage, Manufacturing & Packaging

8.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.

3. Floor life: 168 hours [11] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

[11] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not unpack the modules in large quantities until they are ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.15–0.20 mm. For more details, see ***document [7]***.

The recommended peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

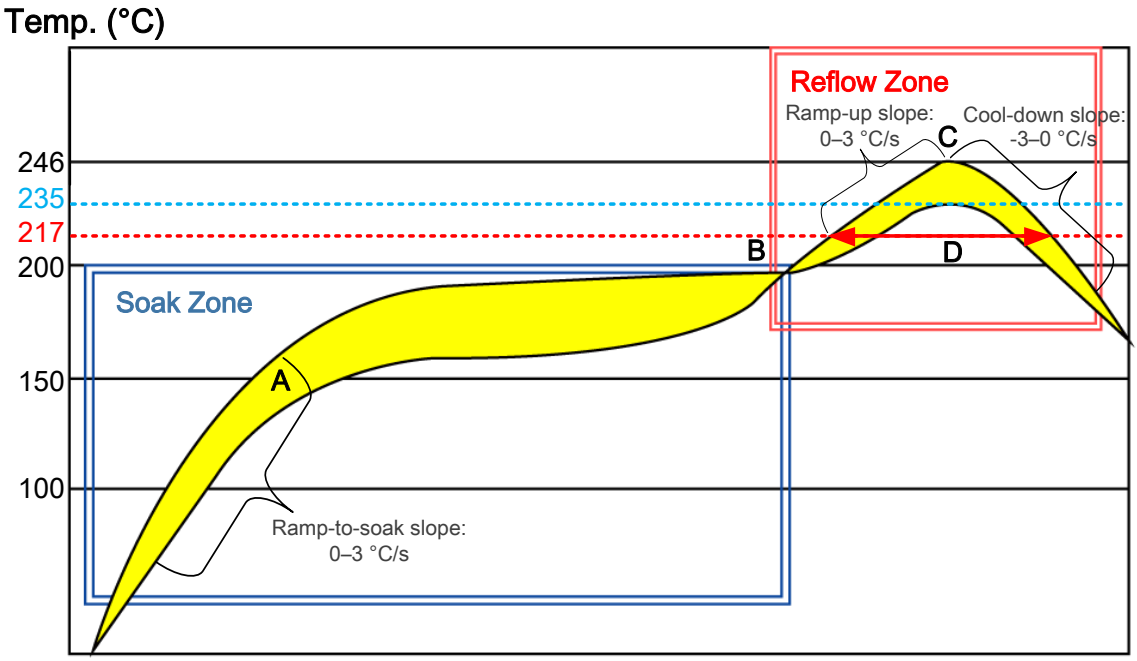


Figure 46: Recommended Reflow Soldering Thermal Profile

Table 44: Recommended Thermal Profile Parameters

Factor	Recommended Value
Soak Zone	
Ramp-to-soak slope	0–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Ramp-up slope	0–3 °C/s
Reflow time (D: over 217 °C)	40–70 s
Max. temperature	235–246 °C
Cool-down slope	-3–0 °C/s
Reflow Cycle	
Max. reflow cycle	1

NOTE

1. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
2. During manufacturing and soldering, or any other processes that may contact the module directly, NEVER wipe the module's shielding can with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol, trichloroethylene, etc. Otherwise, the shielding can may become rusted.
3. The shielding can for the module is made of Cupro-Nickel base material. It is tested that after 12 hours' Neutral Salt Spray test, the laser engraved label information on the shielding can is still clearly identifiable and the QR code is still readable, although white rust may be found.
4. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
5. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
6. Avoid using materials that contain mercury (Hg), such as adhesives, for module processing, even if the materials are RoHS compliant and their mercury content is below 1000 ppm (0.1 %).
7. Due to the complexity of the SMT process, please contact Quectel Technical Support in advance for any situation that you are not sure about, or any process (e.g., selective soldering, ultrasonic soldering) that is not mentioned in ***document [8]***.

8.3. Packaging Specifications

This chapter outlines the key packaging parameters and processes. All figures below are for reference purposes only, as the actual appearance and structure of packaging materials may vary in delivery.

The modules are packed in a tape and reel packaging as specified in the sub-chapters below.

8.3.1. Carrier Tape

Carrier tape dimensions are illustrated in the following figure and table:

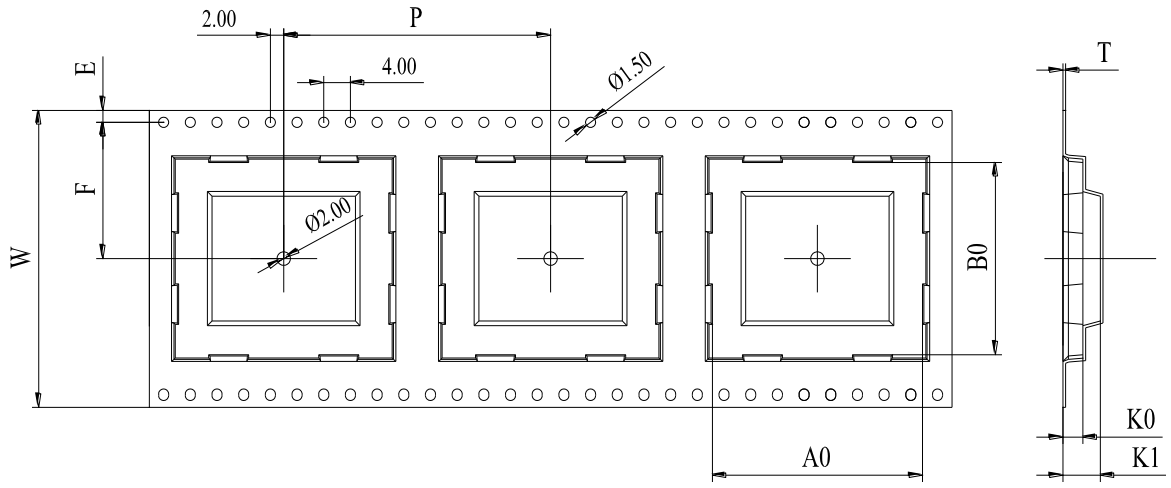


Figure 47: Carrier Tape Dimension Drawing (Unit: mm)

Table 45: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
44	40	0.4	31.5	28.5	3	5.6	20.2	1.75

8.3.2. Plastic Reel

Plastic reel dimensions are illustrated in the following figure and table:

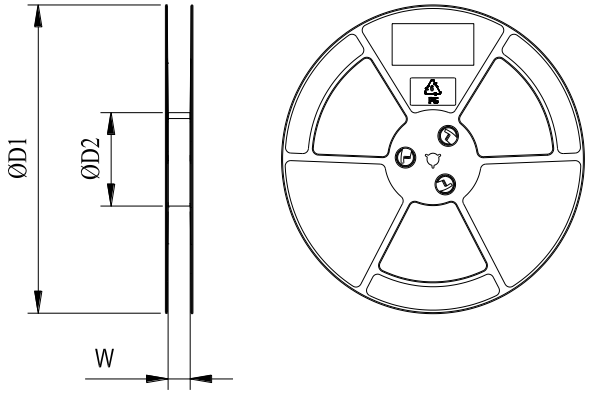


Figure 48: Plastic Reel Dimension Drawing

Table 46: Plastic Reel Dimension Table (Unit: mm)

øD1	øD2	W
330	100	44.5

8.3.3. Mounting Direction

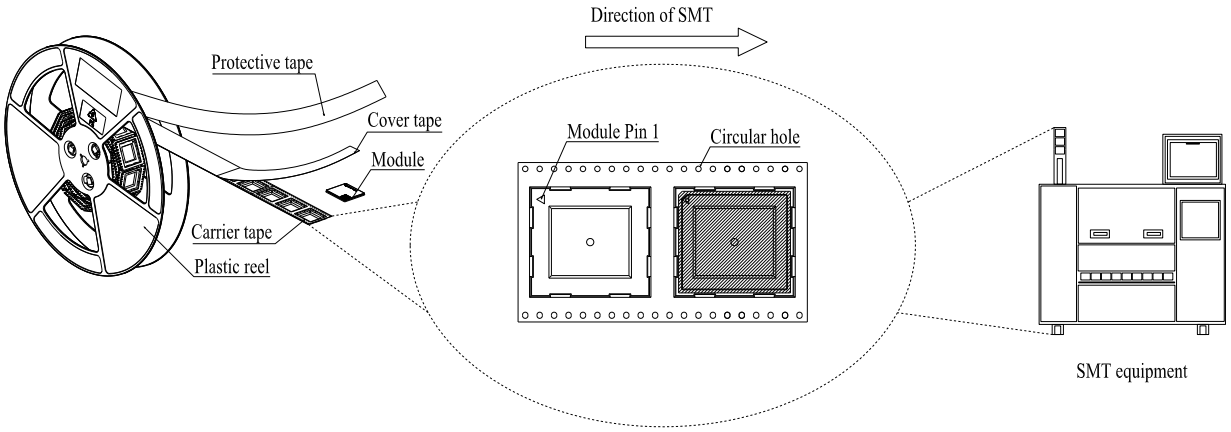
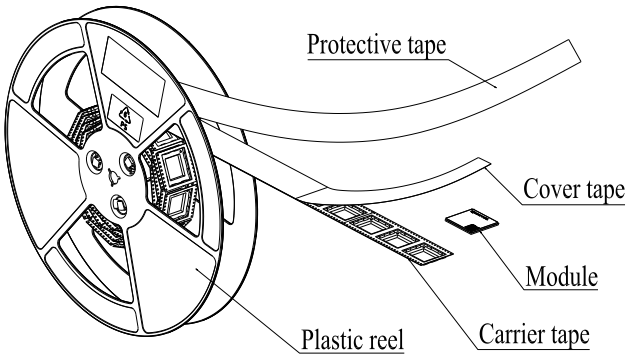


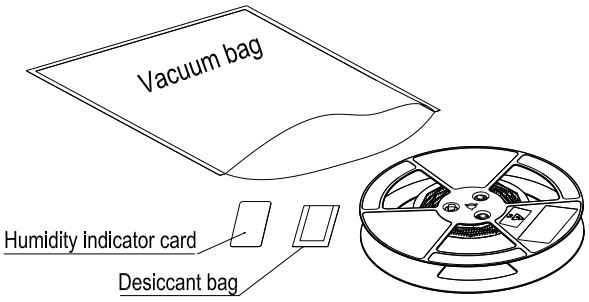
Figure 49: Mounting Direction

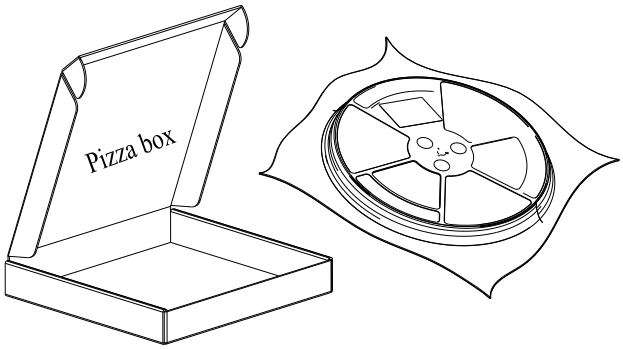
8.3.4. Packaging Process



Place the modules onto the carrier tape cavity and cover them securely with cover tape. Wind the heat-sealed carrier tape onto a plastic reel and apply a protective tape for additional protection. 1 plastic reel can pack 250 modules.

Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, and vacuumize it.





Place the vacuum-packed plastic reel into a pizza box.

Place the 4 packaged pizza boxes into 1 carton and seal it. 1 carton can pack 1000 modules.

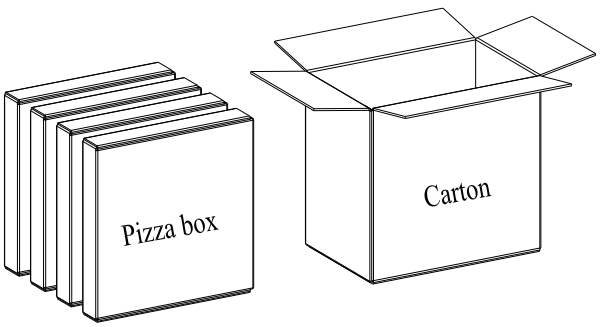


Figure 50: Packaging Process

9 Appendix References

Table 47: Related Documents

Document Name
[1] Quectel_UMTS&LTE_EVB_User_Guide
[2] Quectel_EC200D&ECx00G&EC600U&EG800G_Series_AT_Commands_Manual
[3] Quectel_ECx00G&EC600U&EG800G_Series_Low_Power_Mode_Application_Note
[4] Quectel_ECx00G&EG800G_Series_PWM_Audio_Application_Note
[5] Quectel_EC200G-CN&EG800G-CN_GNSS_Application_Note
[6] Quectel_RF_Layout_Application_Note
[7] Quectel_Module_Stencil_Design_Requirements
[8] Quectel_Module_SMT_Application_Note

Table 48: Terms and Abbreviations

Abbreviation	Description
3GPP	3rd Generation Partnership Project
ADC	Analog-to-Digital Converter
BDS	BeiDou Navigation Satellite System
bps	bits per second
CEP	Circular Error Probable
CHAP	Challenge Handshake Authentication Protocol
CMUX	Connection MUX

CTS	Clear to Send
DTR	Data Terminal Ready
EMI	Electromagnetic Interference
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
ETSI	European Telecommunications Standards Institute
EVB	Evaluation Board
FDD	Frequency Division Duplex
FILE	File Protocol
FOTA	Firmware Over-The-Air
FTP	File Transfer Protocol
FTPS	FTP-over-SSL
GNSS	Global Navigation Satellite System
GPIO	General-Purpose Input/Output
GPS	Global Positioning System
HTTP	Hypertext Transfer Protocol
HTTPS	Hypertext Transfer Protocol over Secure Socket Layer
LCC	Leadless Chip Carrier (package)
LDO	Low-dropout Regulator
LGA	Land Grid Array
LNA	Low-Noise Amplifier
LTE	Long Term Evolution
MCU	Microcontroller Unit/Microprogrammed Control Unit
ME	Mobile Equipment
MLCC	Multi-layer Ceramic Capacitor

MMS	Multimedia Messaging Service
MQTT	Message Queuing Telemetry Transport
MSL	Moisture Sensitivity Levels
NITZ	Network Identity and Time Zone
NMEA	NMEA (National Marine Electronics Association) 0183 Interface Standard
NTP	Network Time Protocol
PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PDU	Protocol Data Unit
PING	Packet Internet Groper
PPP	Point-to-Point Protocol
QZSS	Quasi-Zenith Satellite System
RAM	Random Access Memory
RF	Radio Frequency
RHCP	Right Hand Circular Polarization
RoHS	Restriction of Hazardous Substances
RTS	Require To Send
SDIO	Secure Digital Input/Output Card
SMS	Short Message Service
SMTP	Simple Mail Transfer Protocol
SMTPS	Simple Mail Transfer Protocol Secure
SSL	Secure Sockets Layer
TCP	Transmission Control Protocol
TDD	Time Division Duplexing

TVS	Transient Voltage Suppressor
UART	Universal Asynchronous Receiver & Transmitter
UDP	User Datagram Protocol
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
USB	Universal Serial Bus
USIM	Universal Subscriber Identity Module
Vmax	Maximum Voltage
Vnom	Nominal Voltage
Vmin	Minimum Voltage
V_{IH}	High-level Input Voltage
V_{IL}	Low-level Input Voltage
V_{OH}	High-level Output Voltage
V_{OL}	Low-level Output Voltage
VBAT	Voltage at Battery (Pin)
VSWR	Voltage Standing Wave Ratio